# LXT332

## Dual T1/E1 Line Interface Unit with Crystal-less Jitter Attenuation

## General Description

The LXT332 is a fully integrated Dual Line Interface Unit (DLIU) for both 1.544 Mbps (T1) and 2.048 Mbps (E1) applications. It features B8ZS/HDB3 encoders and decoders, and a constant low output impedance transmitter for high return loss. Transmit pulse shape is selectable for various line lengths and cable types.

The LXT332 incorporates an advanced crystal-less digital jitter attenuator, switchable to either the transmit or receive side. This eliminates the need for an external quartz crystal. It offers both a serial interface (SIO) for microprocessor control and a hardware control mode for stand-alone operation.

The LXT332 offers a variety of advanced diagnostic and performance monitoring features. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

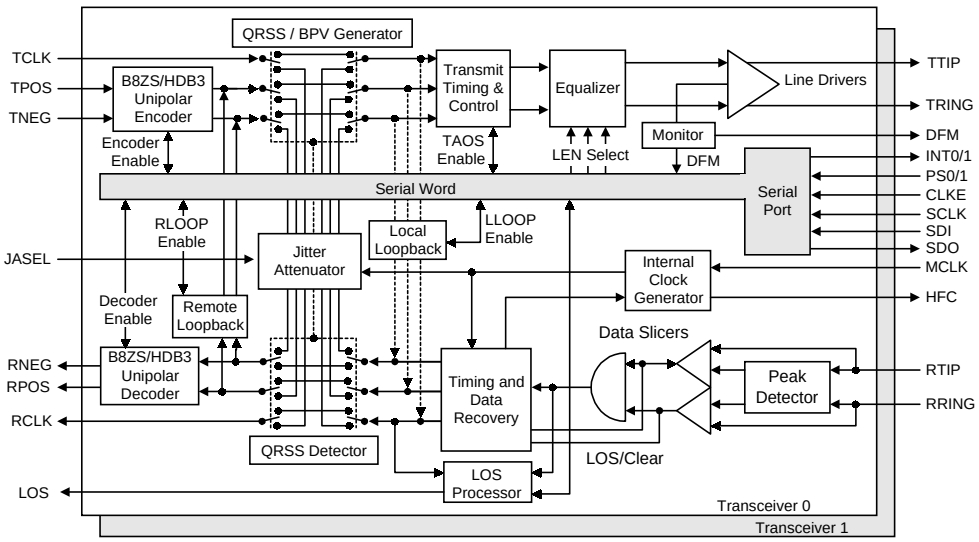
## Applications

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- SONET/SDH Multiplexers
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

## Features

- Digital (crystal-less) jitter attenuation, selectable for receive or transmit path, or may be disabled
- High transmit and receive return loss
- Constant low output impedance transmitter with programmable equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft
- Meets or exceeds industry specifications including ITU G.703, ANSI T1.403 and AT&T Pub 62411
- Compatible with most industry standard framers
- Complete line driver, data recovery and clock recovery functions
- Minimum receive signal of 500 mV, with selectable slicer levels (E1/DSX-1) to improve SNR
- Local, remote, and dual loopback functions
- Built-In Self Test with QRSS Pattern Generator
- Transmit / Receive performance monitors with Driver Fail Monitor (DFM) and Loss of Signal (LOS) outputs
- Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz
- Available in 44-pin PLCC and 44-pin QFP

## LXT332 Block Diagram



# OVERVIEW

In addtion to the inherent advantages of a DLIU, the LXT332 also provides several advanced features which are not available in other LXT30x-series devices. All of the added features are easily implemented. Many require only a clock pulse to change from one mode to another. Some features are available in Host Mode only.

- Two complete LIUs in a single PLCC or QFP package
- Simplifies board design, saves real estate
- Proven architecture (LXT3xx series)
- Crystal-less Jitter Attenuation
- New Features

## Standard LXT332 Features

- **Tri-state Outputs**
  - All LXT332 output pins can be forced to a high-Z Tri-state mode. The Tri-state mode is enabled or disabled by the TRSTE pin.
- **Bipolar or Unipolar Data I/O**
  - The LXT332 / Framer interface can be either bipolar (default) or unipolar (selectable). The unipolar mode is selected by applying MCLK to the TRSTE pin.
- **B8ZS or HDB3 Zero Suppression**
  - The LXT332 incorporates zero suppression encoders and decoders for use in the unipolar data I/O mode. The encoders/decoders can be activated or deactivated by changing the logic level on the remapped TNEG pin.
- **Selectable Jitter Attenuation**
  - Jitter attenuation can be placed in either the transmit or receive path or deactivated. The Jitter Attenuation Select (JASEL) pin determines the jitter attenuation mode. No crystal required.
- **Dual Loopback**
  - This option enables simultaneous loopbacks to both the framer and the line. The TCLK, TPOS and TNEG framer inputs are routed through the jitter attenuator and looped back to the RCLK, RPOS and RNEG outputs. The RTIP/RRING line inputs are looped back through the timing recovery block and line driver onto the TTIP/TRING outputs.

## Additional Host-Mode Features

- **High Frequency Clocks**
  - The LXT332 provides a pair of high frequency clock outputs, one for each LIU. These 8x clocks (12.352 MHz for T1, 16.384 MHz for E1) are tied to the de-jittered clock from the JA of the respective LIU.
- **Bipolar Violation Insertion**
  - The same pins which provide the High Frequency Clocks can also be used to insert bipolar violations into the outgoing data stream. Violations can be inserted into each LIU channel independently.
- **Built-In Self Test (QRSS)**
  - The LXT332 can generate and transmit a QRSS pattern to Built-In Self Test (BIST) applications. Logic errors and bipolar violations can be inserted into the QRSS output. The LXT332 also detects QRSS pattern synchronization and reports bit errors in the received QRSS pattern data stream.
- **AIS Detection**
  - The LXT332 detects the AIS alarm signal on the receive side independent of the loopback modes. When AIS is detected (less than 3 zeros in 2048 bits), the LXT332 provides an indicator output.

# PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figures 1 and 2 show the pinout diagrams for the PLCC and QFP packages, respectively. Table 1 describes the Host Mode signal functions, except signals that change when in Unipolar Host Mode. Table 2 describes signal functions that change when in Unipolar Most Mode. Table 3 describes all Hardware Mode signal functions, except signals that change when in Unipolar Mode. Table 4 describes signal functions that change when in Unipolar Hardware Mode.

**Figure 1: LXT332 Pin Assignments (PLCC Package)**

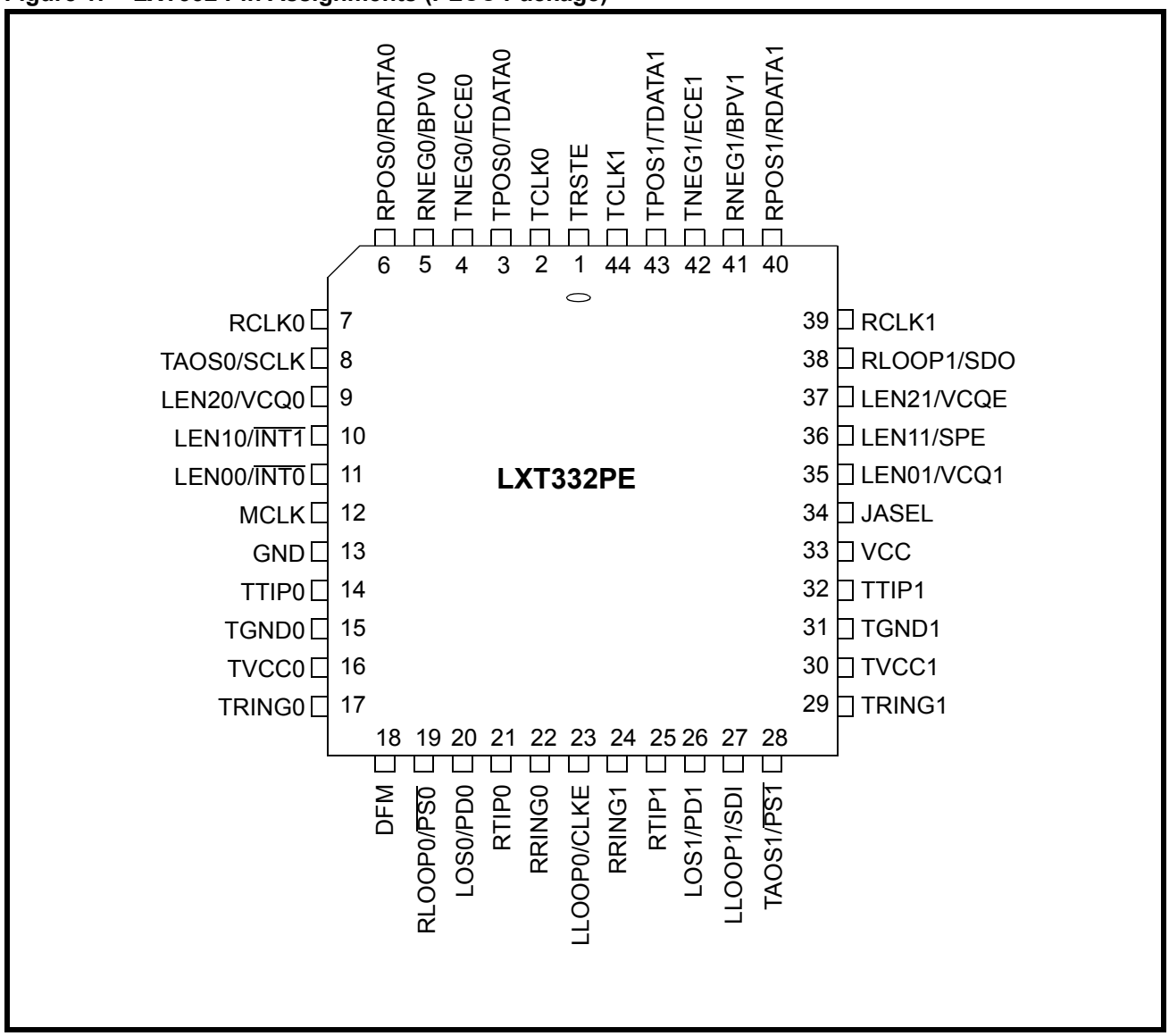


**Figure 2: LXT332 Pin Assignments (QFP Package)**

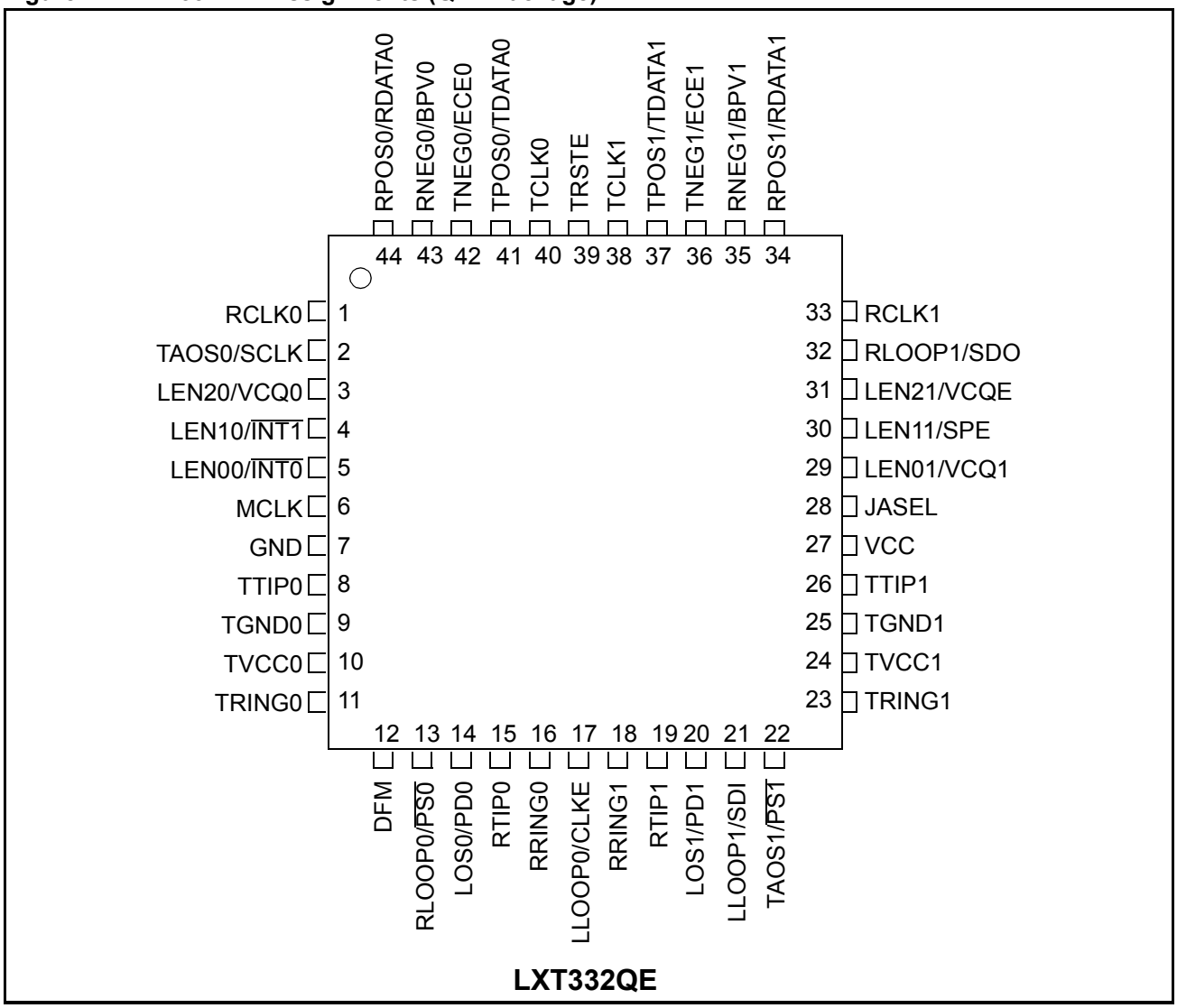



**Table 1: Host Mode Pin and Bipolar Host Mode Pin Descriptions**

| Pin QFP | Pin PLCC | Symbol | I/O[1] | Description |
|---|---|---|---|---|
| 39 | 1 | TRSTE | DI | **Tristate Output Enable Input Pin.** Forces all output pins to high-Z tri-state when held High. Enables Bipolar I/O mode when held Low. In this mode the framer interface is bipolar (TPOS/TNEG and RPOS/RNEG), and the B8ZS/HDB3 encoders are disabled. Enables Unipolar I/O mode when clocked by MCLK. In this mode the framer interface is unipolar (TDATA and RDATA), and the TNEG and RNEG pins are re-mapped. The TNEG pins are re-mapped as Encoder Enable (ECE) to individually enable the B8ZS/HDB3 encoder/decoder for each port. The RNEG pins are re-mapped as Bipolar Violation (BPV) indicators to report BPVs received at the respective ports. |
| 40 | 2 | TCLK0 | DI | **Transmit Clock - Port 0.** 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK. |

1 DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

**Table 1: Host Mode Pin and Bipolar Host Mode Pin Descriptions** – continued

| Pin QFP | Pin PLCC | Symbol | I/O[1] | Description |
|---|---|---|---|---|
| 41 | 3 | TPOS0 (Bipolar) | DI | **Transmit Positive and Negative Data - Port 0.** In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar input pair for port 0. Data to be transmitted onto the twisted-pair line is input at these pins. However, when the TRSTE pin is clocked by MCLK, the LXT332 switches to a unipolar mode. Table 2 describes Unipolar mode pin functions. |
| 42 | 4 | TNEG0 (Bipolar) | DI | |
| 43 | 5 | RNEG0 (Bipolar) | DO | **Receive Positive and Negative Data - Port 0.** In the Bipolar I/O mode, these pins are the data outputs from port 0. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). In Host mode, CLKE determines the clock edge at which these outputs are stable and valid. |
| 44 | 6 | RPOS0 (Bipolar) | DO | |
| 1 | 7 | RCLK0 | DO | **Receive Clock - Port 0.** This clock is recovered from the input signal. Under Loss of Signal (LOS) conditions, this output is derived from MCLK. |
| 2 | 8 | SCLK | DI | **Serial Clock.** The Serial Clock shifts data into or out from the serial interface register of the selected port. |
| 3 | 9 | VCQ0 | DI/O | Provides Violation insert, High Frequency Clock, or QRSS generation/detection functions for Port 0. Pin operation is determined by the VCQE pin.<br><br>**Violation Insertion Function.** When the **V**iolation insertion function is enabled, this pin is sampled on the falling edge of TCLK to control bipolar violation (BPV) insertion. If High, a BPV is inserted at the next available mark transmitted from port 0. A Low-to-High transition is required for each subsequent violation insertion. (B8ZS and HDB3 zero suppression codes are not violated.)<br><br>**Clock Function.** When the **C**lock function is enabled, this pin outputs a High Frequency Clock (12.352 MHz for T1, 16.384 MHz for E1) tied to the jitter attenuated clock of port 0. If no JA clock is available, HFC is locked to the 8x receive timing recovery clock.<br><br>**Quasi Random Signal Source (QRSS) Function.** When the QRSS function is enabled, a High on this pin enables the QRSS detection circuit and causes the LXT332 to transmit the QRSS pattern onto the twisted-pair line from port 0. For error-free QRSS transmission, TPOS0 must be held Low. To insert errors into the pattern, TPOS must transition from Low to High (TPOS is sampled on the falling edge of MCLK). A Low-to-High transition is required for each subsequent violation insertion. (B8ZS and HDB3 zero suppression codes are not violated.) |
| 4 | 10 | $\overline{\text{INT1}}$ | DO | **Interrupt Outputs.** The interrupt outputs go Low to flag the host processor that the respective port has changed state. INT0 and INT1 are open drain outputs. Each must be tied to VCC through a resistor. |
| 5 | 11 | $\overline{\text{INT0}}$ | DO | |
| 6 | 12 | MCLK | DI | **Master Clock.** The master clock (1.544 MHz for T1, 2.048 MHz for E1) input must be independent, free-running, continuously active and jitter free for receiver operation. Since the transceivers derive their RCLK timing from the MCLK input on Loss of Signal (LOS), MCLK cannot be derived from RCLK. |
| 7 | 13 | GND | – | **Ground.** Ground return for power supply VCC. |

1 DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

**Table 1: Host Mode Pin and Bipolar Host Mode Pin Descriptions** – continued

| Pin QFP | Pin PLCC | Symbol | I/O[1] | Description |
|---|---|---|---|---|
| 8<br>11 | 14<br>17 | TTIP0<br>TRING0 | AO<br>AO | **Transmit Tip and Ring - Port 0.** The tip and ring pins for each port are differential driver outputs designed to drive a 35 - 200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height. See Figures 19 through 21. |
| 9 | 15 | TGND0 | – | **Ground.** Ground return for power supply TVCC0. |
| 10 | 16 | TVCC0 | I | **+ 5 volt power supply input for the port 0 transmit driver.** TVCC0 must not vary from TVCC1 or VCC by more than ± 0.3 V. |
| 12 | 18 | DFM | O | **Driver Fail Monitor.** This signal goes High to indicate a driver output short in one or both ports. |
| 13 | 19 | $\overline{PS0}$ | I | **Port Select - Port 0.** This input accesses the serial interface registers for port 0. For each read or write operation, PS must transition from High to Low, and remain Low. |
| 14 | 20 | PD0 | DO | **Pattern Detect - Port 0.** Unless the QRSS function is selected by the VCQE pin, PD0 functions as an AIS alarm indicator. The AIS pattern is detected by the receiver, independent of any loopback mode. AIS goes High when less than three zeros have been detected in any string of 2048 bits. AIS returns Low when the received signal contains more than three zeros in 2048 bits. (LOS is available via the SIO register and interrupt.)<br><br>If the QRSS function is enabled by the VCQE pin, PD0 remains High until pattern sync is reached with the received signal. Once pattern lock is obtained, PD0 goes Low. (The sync/out-of-sync criteria is less than 3/4 errors in 128 bits.) After sync acquisition, bit errors cause PD0 to go High for half a clock cycle. This output can be used to trigger an external error counter. |
| 15<br>16 | 21<br>22 | RTIP0<br>RRING0 | DI<br>DI | **Receive Tip and Ring - Port 0.** RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a center-tapped 1:2 transformer. |
| 17 | 23 | CLKE | DI | **Clock Edge Select.** When CLKE is High, RPOS/RNEG or RDATA outputs are valid on the falling edge of RCLK, and SDO is valid on the rising edge of SCLK. When CLKE is Low, RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK. |
| 18<br>19 | 24<br>25 | RRING1<br>RTIP1 | AI<br>AI | **Receive Tip and Ring - Port 1.** RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a center-tapped 1:2 transformer. |
| 20 | 26 | PD1 | DO | **Pattern Detect - Port 1.** Reports AIS and QRSS pattern reception. See PD0 signal description for details. |
| 21 | 27 | SDI | DI | **Serial Data Input.** SDI is sampled on the rising edge of SCLK. |
| 22 | 28 | $\overline{PS1}$ | DI | **Port Select - Port 1.** This input accesses the serial interface registers for port 1. For each read or write operation, PS must transition from High to Low, and remain Low. |
| 23<br>26 | 29<br>32 | TRING1<br>TTIP1 | AO<br>AO | **Transmit Tip and Ring - Port 1.** The tip and ring pins for each port are differential driver outputs designed to drive a 35 - 200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height. See Figures 13 through 15. |

1 DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

**Table 1: Host Mode Pin and Bipolar Host Mode Pin Descriptions** – continued

| Pin QFP | Pin PLCC | Symbol | I/O[1] | Description |
|---|---|---|---|---|
| 24 | 30 | TVCC1 | AI | **+ 5 volt power supply input for the port 1 transmit driver.** TVCC1 must not vary from TVCC0 or VCC by more than ± 0.3 V. |
| 25 | 31 | TGND1 | – | **Ground.** Ground return for power supply TVCC1. |
| 27 | 33 | VCC | AI | **+5 VDC power supply** input for all circuits, except the transmit drivers. |
| 28 | 34 | JASEL | DI | **Jitter Attenuation Select.** Selects jitter attenuation for both ports. When JASEL = 1, JA circuits are placed in the receive paths. When JASEL = 0, JA circuits are placed in the transmit paths. When JASEL is clocked with MCLK, the JA circuit is disabled. |
| 29 | 35 | VCQ1 | DI/O | **Violation insert, Clock, or QRSS.** Function (Violation insert, Clock, or QRSS) is determined by the VCQE pin. Provides Violation Insertion, High Frequency Clock or QRSS Generation functions for Port 1. Refer to VCQ0 signal description for details. |
| 30 | 36 | SPE | DI | **Serial Port Enable.** SPE must be clocked with MCLK to enable Host Mode control through the serial port. |
| 31 | 37 | VCQE | DI | **Violation - Clock - QRSS Enable.** When set High, enables the Bipolar Violation Insert functions of VCQ0 and VCQ1 pins. When set Low, enables the High Frequency Clock functions of VCQ0 and VCQ1. When clocked with MCLK, enables the QRSS functions of VCQ0 and VCQ1, and enables the QRSS Generate and Detect function of PD0 and PD1 pins. |
| 32 | 38 | SDO | DO | **Serial Data Output.** If CLKE is High, SDO is valid on the rising edge of SCLK. If CLKE is Low, SDO is valid on the falling edge of SCLK. |
| 33 | 39 | RCLK1 | DO | **Receive Clock - Port 1.** This clock is recovered from the input signal. Under Loss of Signal (LOS) conditions, this output is derived from MCLK. |
| 34<br><br>35 | 40<br><br>41 | RPOS1 (Bipolar)<br><br>RNEG1 (Bipolar) | DO<br><br>DO | **Receive Positive and Negative Data - Port 1.** In the Bipolar I/O mode, these pins are the data outputs from port 1. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). CLKE determines the clock edge at which these outputs are stable and valid. |
| 36<br><br>37 | 42<br><br>43 | TNEG1 (Bipolar)<br><br>TPOS1 (Bipolar) | DI<br><br>DI | **Transmit Positive and Negative Data - Port 1.** In the Bipolar I/O mode, these pins are TPOS and TNEG, the positive and negative sides of a bipolar input pair for port 1. Data to be transmitted onto the twisted-pair line is input at these pins. However, when TRSTE is clocked by MCLK, the LXT332 switches to a unipolar mode. Unipolar mode pin functions are described separately. |
| 38 | 44 | TCLK1 | DI | **Transmit Clock - Port 1.** 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK. |

1 DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

**Table 2: Unipolar Host Mode Pin Descriptions[1]**

| Pin QFP | Pin PLCC | Symbol | I/O | Description |
|---|---|---|---|---|
| 41 | 3 | TDATA0 | DI | **Transmit Data - Port 0.** In the Unipolar mode, the data to be transmitted onto the twisted-pair line from port 0 is input at this pin. |

1 Table 1 describes the pins that do not change function in Unipolar Host Mode and functions of pins unique to Bipolar Mode.

**Table 2: Unipolar Host Mode Pin Descriptions[1]** – continued

| Pin QFP | Pin PLCC | Symbol | I/O | Description |
|---|---|---|---|---|
| 42 | 4 | ECE0 | DI | **Encoder Enable - Port 0.** In the Unipolar mode, a High on this pin enables the B8ZS or HDB3 encoder and decoder for port 0. |
| 43 | 5 | BPV0 | DO | **Bipolar Violation - Port 0.** In the Unipolar mode this indicator output goes High when a bipolar violation is received at port 0. |
| 44 | 6 | RDATA0 | DO | **Receive Data - Port 0.** In the Unipolar mode, RDATA is a Non-Return-to-Zero (NRZ) output. CLKE determines the RCLK edge which RDATA is stable and valid. |
| 34 | 40 | RDATA1 | DO | **Receive Data - Port 1.** In the Unipolar mode, RDATA is a Non-Return-to-Zero (NRZ) output. CLKE determines the RCLK edge which RDATA is stable and valid. |
| 35 | 41 | BPV1 | DO | **Bipolar Violation - Port 1.** In the Unipolar mode this indicator output goes High when a bipolar violation is received at port 1. |
| 36 | 42 | ECE1 | DI | **Encoder Enable - Port 1.** In the Unipolar mode, a High on this pin enables the B8ZS or HDB3 encoder and decoder for port 1. |
| 37 | 43 | TDATA1 | DI | **Transmit Data - Port 1.** In the Unipolar mode, the data to be transmitted onto the twisted-pair line from port 1 is input at this pin. |

1 Table 1 describes the pins that do not change function in Unipolar Host Mode and functions of pins unique to Bipolar Mode.

**Table 3: Hardware Mode Pin and Bipolar Hardware Mode Pin Descriptions[1]**

| Pin QFP | Pin PLCC | Symbol | I/O[2] | Description |
|---|---|---|---|---|
| 39 | 1 | TRSTE | DI | **Tristate Output Enable Input Pin.** Forces all output pins to high-Z Tri-state when held High. Enables Bipolar I/O mode when held Low. In this mode the framer interface is bipolar (TPOS/TNEG and RPOS/RNEG), and the B8ZS/HDB3 encoders are disabled. Enables Unipolar I/O mode when clocked by MCLK. In this mode the framer interface is unipolar (TDATA and RDATA), and the TNEG and RNEG pins are re-mapped. The TNEG pins are re-mapped as Encoder Enable (ECE) to individually enable the B8ZS/HDB3 encoder/decoder for each port. The RNEG pins are re-mapped as Bipolar Violation (BPV) indicators to report BPVs received at the respective ports. |
| 40 | 2 | TCLK0 | DI | **Transmit Clock - Port 0.** 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK. |
| 41<br><br>42 | 3<br><br>4 | TPOS0 (Bipolar)<br><br>TNEG0 (Bipolar) | DI | **Transmit Data Positive and Negative - Port 0.** In the Bipolar I/O mode, these pins are the positive and negative sides of a bipolar input pair for port 0. Data to be transmitted onto the twp line is input at these pins. However, when TRSTE is clocked by MCLK, the LXT332 switches to a unipolar mode. Unipolar mode pin functions are described separately. |
| 43<br><br>44 | 5<br><br>6 | RNEG0 (Bipolar)<br><br>RPOS0 (Bipolar) | DO | **Receive Data Positive and Negative - Port 0.** In the Bipolar I/O mode, a signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). RPOS and RNEG are stable and valid on the rising edge of RCLK. |

1 Table 4 describes the pins used in Unipolar Hardware Mode.
2. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

**Table 3: Hardware Mode Pin and Bipolar Hardware Mode Pin Descriptions[1]** – continued

| Pin QFP | Pin PLCC | Symbol | I/O[2] | Description |
|---|---|---|---|---|
| 1 | 7 | RCLK0 | DO | **Receive Clock - Port 0.** This clock is recovered from the input signal. Under Loss of Signal (LOS) conditions, this output is derived from MCLK. |
| 2 | 8 | TAOS0 | DI | **Transmit All Ones Enable - Port 0.** When TAOS is High and RLOOP is Low, the TPOS/TNEG or TDATA input is ignored and port 0 transmits a stream of ones at the TCLK frequency. If TCLK is not provided, the MCLK input is used as the transmit reference. |
| 3<br>4<br>5 | 9<br>10<br>11 | LEN20<br>LEN10<br>LEN00 | DI<br>DI<br>DI | **Line Length Equalizer Inputs - Port 0.** This pins determine the shape and amplitude of the transmit pulse. |
| 6 | 12 | MCLK | DI | **Master Clock.** The master clock (1.544 MHz for T1, 2.048 MHz for E1) input must be independent, free-running, continuously active and jitter free for receiver operation. Since the transceivers derive their RCLK timing from the MCLK input on Loss of Signal (LOS), MCLK cannot be derived from RCLK. |
| 7 | 13 | GND | – | **Ground.** Ground return for power supply VCC. |
| 8<br>11 | 14<br>17 | TTIP0<br>TRING0 | AO<br>AO | **Transmit Tip and Ring - Port 0.** The tip and ring pins for each port are differential driver outputs designed to drive a 35 - 200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height. See Figures 13 through 15. |
| 9 | 15 | TGND0 | – | **Ground.** Ground return for power supply TVCC0. |
| 10 | 16 | TVCC0 | AI | **+ 5 volt** power supply input for the port 0 transmit driver. TVCC0 must not vary from TVCC1 or VCC by more than ± 0.3 V. |
| 12 | 18 | DFM | DO | **Driver Fail Monitor.** This signal goes High to indicate a driver output short in one or both ports. |
| 13 | 19 | RLOOP0 | DI | **Remote Loopback Enable - Port 0.** When RLOOP = 1, the port 0 clock and data inputs from the framer are ignored and the data received from the twisted-pair line is transmitted back onto the line at the RCLK frequency. **(LLOOP0 must be Low for RLOOP0 to occur.)** |
| 14 | 20 | LOS0 | DO | **Loss of Signal - Port 0.** LOS goes High when 175 consecutive spaces have been detected. LOS returns Low when the received signal reaches a mark density of 12.5% (determined by receipt of four marks with a sliding 32-bit period with no more than 15 consecutive zeros). Received marks are output on RPOS/RNEG or RDATA even when LOS is High. |
| 15<br>16 | 21<br>22 | RTIP0<br>RRING0 | AI<br>AI | **Receive Tip and Ring - Port 0.** RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a center-tapped 1:2 transformer. |
| 17 | 23 | LLOOP0 | DI | **Local Loopback Enable - Port 0.** When LLOOP is High, the RTIP/RRING inputs from the port 0 line are disconnected and the transmit data inputs are routed back into the receive inputs (through JA if enabled). **(RLOOP0 must be Low for LLOOP0 to occur.)** |
| 18<br>19 | 24<br>25 | RRING1<br>RTIP1 | AI<br>AI | **Receive Tip and Ring - Port 1.** RTIP and RRING comprise the receive line interface. This input pair should be connected to the line through a center-tapped 1:2 transformer. |

1 Table 4 describes the pins used in Unipolar Hardware Mode.
2. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

**Table 3: Hardware Mode Pin and Bipolar Hardware Mode Pin Descriptions[1]** – continued

| Pin QFP | Pin PLCC | Symbol | I/O[2] | Description |
|---|---|---|---|---|
| 20 | 26 | LOS1 | DO | **Loss of Signal - Port 1.** LOS goes High when 175 consecutive spaces have been detected. LOS returns to a logic 0 when the received signal reaches a mark density of 12.5% (refer to LOS0 signal description for details). |
| 21 | 27 | LLOOP1 | DI | **Local Loopback Enable - Port 1. (RLOOP1 must be Low for LLOOP1 to occur.)** |
| 22 | 28 | TAOS1 | DI | **Transmit All Ones Enable - Port 1. (RLOOP1 must be Low for TAOS1 to occur.)** |
| 23<br>26 | 29<br>32 | TRING1<br>TTIP1 | AO<br>AO | **Transmit Ring - Port 1.** The tip and ring pins for each port are differential driver outputs designed to drive a 35 - 200 Ω load. Line matching resistors and transformers can be selected to give the desired pulse height. See Figures 19 through 21. |
| 24 | 30 | TVCC1 | AI | **+ 5 volt** power supply input for the port 1 transmit driver. TVCC1 must not vary from TVCC0 or VCC by more than ± 0.3 V. |
| 25 | 31 | TGND1 | – | **Ground.** Ground return for power supply TVCC1. |
| 27 | 33 | VCC | AI | **+5 VDC** power supply input for all circuits, except the transmit drivers. |
| 28 | 34 | JASEL | DI | **Jitter Attenuation Select.** Selects jitter attenuation for both ports. When JASEL = 1, JA circuits are placed in the receive paths. When JASEL = 0, JA circuits are placed in the transmit paths. When JASEL is clocked with MCLK, the JA circuit is disabled. |
| 29<br>30<br>31 | 35<br>36<br>37 | LEN01<br>LEN11<br>LEN21 | DI<br>DI<br>DI | **Line Length Equalizer inputs - Port 1.** These pins determine the shape and amplitude of the transmit pulse. |
| 32 | 38 | RLOOP1 | DI | **Remote Loopback Enable - Port 1. (LLOOP1 must = 0 for RLOOP to occur.)** |
| 33 | 39 | RCLK1 | DO | **Receive Clock - Port 1.** This clock is recovered from the twisted-pair input signal. Under Loss of Signal (LOS) conditions, this output is derived from MCLK. |
| 34<br>35 | 40<br>41 | RPOS1 (Bipolar)<br>RNEG1 (Bipolar) | DO<br>DO | **Receive Data Positive and Negative - Port 1.** In the Bipolar I/O mode, these pins are the data outputs from port 1. A signal on RPOS corresponds to receipt of a positive pulse on RTIP/RRING. A signal on RNEG corresponds to receipt of a negative pulse on RTIP/RRING. RNEG/RPOS outputs are Non-Return-to-Zero (NRZ). RPOS and RNEG are stable and valid on the rising edge of RCLK. |
| 36<br>37 | 42<br>43 | TNEG1<br>TPOS1 | DI<br>DI | **Transmit Data Positive and Negative - Port 1.** In the Bipolar I/O mode, these pins are TPOS and TNEG, the positive and negative sides of a bipolar input pair for port 1. Data to be transmitted onto the twisted-pair line is input at these pins. However, when the TRSTE pin is clocked by MCLK, the LXT332 switches to a unipolar mode. Unipolar mode pin functions are described separately. |
| 38 | 44 | TCLK1 | DI | **Transmit Clock - Port 1.** 1.544 MHz for T1, 2.048 MHz for E1. The transmit data inputs are sampled on the falling edge of TCLK. |

1 Table 4 describes the pins used in Unipolar Hardware Mode.
2. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output

**Table 4: Unipolar Hardware Mode Pin Descriptions[1]**

| Pin QFC | Pin PLCC | Symbol | I/O | Description |
|---|---|---|---|---|
| 41 | 3 | TDATA0 | DI | **Transmit Data - Port 0.** In the Unipolar mode, the data to be transmitted onto the line from port 0 is input at this pin. |
| 42 | 4 | ECE0 | DI | **Encoder Enable - Port 0.** In the Unipolar mode, a High on this pin enables the B8ZS or HDB3 encoder and decoder for port 0. |
| 43 | 5 | BPV0 | DO | **Bipolar Violation - Port 0.** In the Unipolar mode this indicator output goes High when a bipolar violation is received at port 0. |
| 44 | 6 | RDATA0 | DO | **Receive Data - Port 0.** In the Unipolar mode, RDATA is a Non-Return-to-Zero (NRZ) output. RDATA is stable and valid on the rising edge of RCLK. |
| 34 | 40 | RDATA1 | DO | **Receive Data - Port 1.** In the Unipolar mode, RDATA is a Non-Return-to-Zero (NRZ) output. RDATA is stable and valid on the rising edge of RCLK. |
| 35 | 41 | BPV1 | DO | **Bipolar Violation - Port 1.** In the Unipolar mode this indicator output goes High when a bipolar violation is received at port 1. |
| 36 | 42 | ECE1 | DI | **Encoder Enable - Port 1.** In the Unipolar mode, a High on this pin enables the B8ZS or HDB3 encoder and decoder for port 1. |
| 37 | 43 | TDATA1 | DI | **Transmit Data - Port 1.** In the Unipolar mode, the data to be transmitted onto the line from port 1 is input at this pin. |

1 Table 3 describes the pins that do not change function in Unipolar Hardware Mode and the functions of pins unique to Bipolar Mode.

# FUNCTIONAL DESCRIPTION

The figure at the beginning of this Data Sheet shows a simplified block diagram of the LXT332. The LXT332 is a fully integrated Dual Line Interface Unit (DLIU) which contains two complete transceivers. The DLIU is designed for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. Both transceivers operate at the same frequency, which is determined by the MCLK input.

Each DLIU transceiver front end interfaces with two twisted-pair lines, one pair for transmit, one pair for receive. These two twisted-pair lines comprise a digital data loop for full duplex transmission. The integrated crystal-less jitter attenuator may be positioned in either the transmit or receive path, or disabled.

Each DLIU transceiver back-end interfaces with a framer through either bipolar or unipolar data I/O channels. The DLIU may be controlled by a microprocessor through the serial port (Host control mode), or by hard-wired pins for stand-alone operation (Hardware control mode).

## Receiver

The two receivers in the LXT332 DLIU are identical. The following paragraphs describe the operation of one.

The twisted-pair input is received via a center-tapped 1:2 transformer. Positive pulses are received at RTIP, negative pulses at RRING. Recovered data is output at RPOS and RNEG in the bipolar mode and at RDATA in the unipolar mode. The recovered clock is output at RCLK. RPOS/RNEG or RDATA outputs are valid on the rising edge of RCLK. Refer to the Test Specifications Section for receiver timing.

The receive signal is processed through the peak detector and data slicers. The peak detector samples the received signal and determines its maximum value. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (line length inputs LEN0 - LEN2 ≠ 000 or 001) the threshold is set to 70% (typical) of the peak value. This threshold is maintained above the specified level for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (LEN inputs = 000 or 001), the threshold is 50 % (typical).

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of 0.3 V (typical) to provide immunity from impulsive noise.

After processing through the data slicers, the received signal goes to the data and timing recovery section, and to the receive monitor. The data and timing recovery circuits provide an input jitter tolerance better than required by Pub 62411 or ITU G.823, as shown in Test Specifications.

The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS flag is set, and the recovered clock is replaced by MCLK at the RCLK output in a smooth transition. (MCLK is required for receive operation.) When the received signal reaches 12.5% ones density (4 marks in a sliding 32-bit period) with no more than 15 consecutive zeros, the LOS flag is reset and another smooth transition replaces MCLK with the recovered clock at RCLK. During LOS conditions, received data is output on RPOS/RNEG (or RDATA if unipolar I/O is selected).

Depending on the options selected, recovered clock and data signals may be routed through the jitter attenuator, through the B8ZS/HDB3 decoder, and may be output to the framer as either bipolar or unipolar data. In unipolar data I/O mode, the LXT332 reports bipolar violations via an output for one RCLK period on the respective BPV pin.

## Transmitter

The two transmitters in the LXT332 DLIU are identical. The following paragraphs describe the operation of a single transmitter.

Transmit data from the framer is clocked serially into the device at TPOS/TNEG in the bipolar mode or at TDATA in the unipolar mode. The transmit clock (TCLK) supplies the input synchronization. The transmitter samples TPOS/TNEG or TDATA inputs on the falling edge of TCLK. If TCLK is not supplied, the transmitter remains powered down and the TTIP/TRING outputs are held in a high-Z state, except during RLOOP, DLOOP, QRSS or TAOS modes. A separate power supply (TVCC0 or TVCC1) supplies each output driver. Current limiters on the output drivers provide short circuit protection. Refer to the Test Specifications Section for MCLK and TCLK timing characteristics. The LXT332 transmits data as a 50% AMI line code as shown in Figure 3. Enabling the zero suppression encoders/decoders overrides the default and the transmission complies with the selected encoding scheme.

Zero suppression is available only in Unipolar Mode. The two zero-suppression types are B8ZS, used in T1 environ-

ments, and HDB3, used in E1 environments. The scheme selected depends on whether the application is T1 or E1.

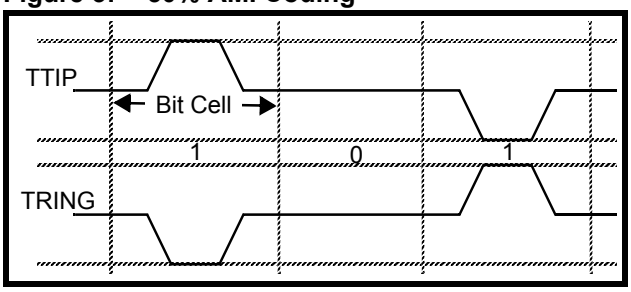
## Bipolar Violation Insertions

In the Host mode with unipolar data I/O selected, a Bipolar Violation (BPV) insert function is available. When the VCQE pin is held High, VCQ0 and VCQ1 pins control bipolar Violation Insertion (VI) for ports 0 and 1, respectively. TDATA and VI are both sampled on the falling edge of TCLK. If VI is High, the next available mark is transmitted as a BPV, except as follows:

1. B8ZS and HDB3 zero suppression is not violated.
2. If Local Loopback (LLOOP) and Transmit All Ones (TAOS) are both active, the BPV is looped back to RDATA but the line driver transmits All Ones (no violations).
3. During Remote Loopback (RLOOP = 1), BPV Insert is disabled.

A Low-to-High transition on VI is required for each subsequent BPV insertion.

**Figure 3: 50% AMI Coding**




## Pulse Shape

The transmitted pulse shape is determined by Line Length equalizer control signals LEN0 through LEN2 as shown in Table 5. Equalizer codes are hardwired in Hardware mode. In Host mode the LEN codes are input through the serial interface. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. The line driver provides a constant low output impedance of < 3Ω (typical), regardless of whether it is driving marks or spaces. This well controlled impedance provides excellent return loss when used with external precision resistors (± 1 % accuracy) in series with the transformer. Table 8 lists recommended transformer specifications. The Application Information Section lists transformer specifications, recommended transformer ratios, series resistor (Rt) values, and typical return losses for various LEN codes. To minimize power consumption the LXT332 can be tied directly to a 1:1.15 transformer without series resistors.

Pulses can be shaped for either 1.544 Mbps or 2.048 Mbps applications. 1.544 Mbps pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of 22 AWG ABAM cable. A combination of 9.1 Ω resistors and a 1:2.3 transformer is recommended for DSX-1 applications. The LXT332 also matches FCC pulse mask specifications for CSU applications.

The LXT332 produces 2.048 Mbps pulses for both 75Ω coaxial (2.37 V) or 120Ω shielded (3.0 V) lines through an output transformer with a 1:2 turns ratio. For coaxial systems, 9.1 Ω series resistors are recommended. For twisted-pair lines, use 15 Ω resistors.

**Table 5: Equalizer Control Inputs**

| LEN2 | LEN1 | LEN0 | Line Length[1] | Cable Loss[2] | Application | Transmit Rate |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 – 133 ft. ABAM | 0.6 dB | DSX-1 | 1.544 Mbps |
| 1 | 0 | 0 | 133 – 266 ft ABAM | 1.2 dB | | |
| 1 | 0 | 1 | 266 – 399 ft ABAM | 1.8 dB | | |
| 1 | 1 | 0 | 399 – 533 ft ABAM | 2.4 dB | | |
| 1 | 1 | 1 | 533 – 655 ft ABAM | 3.0 dB | | |
| 0 | 0 | 0 | ITU Recommendation G.703 | | E1 – Coax (75Ω) | 2.048 Mbps |
| 0 | 0 | 1 | | | E1 – Twisted-pair (120Ω) | |
| 0 | 1 | 0 | FCC Part 68, Option A | | CSU | 1.544 Mbps |

1 Line length from LXT332 to DSX-1 cross-connect point
2. Maximum cable loss at 772 kHz

## Driver Failure Monitor

The transceiver incorporates an internal Driver Failure Monitor (DFM) in parallel with TTIP and TRING. A capacitor, charged via a measure of the driver output current and discharged by a measure of the maximum allowable current detects driver failure. Shorted lines draw excess current, overcharging the cap. When the capacitor charge deviates outside the nominal charge window, a driver fail is reported. In Host mode the DFM bit is set in the serial word. In Hardware mode the DFM pin goes High. During a long string of spaces, a short-induced overcharge eventually bleeds off, clearing the DFM flag.

## Jitter Attenuation

A digital Jitter Attenuation Loop (JAL) combined with an Elastic Store (ES) provides Jitter attenuation. The JAL is internal and requires no external crystal nor high-frequency (higher than line rate) clock. When JASEL = 1, the JAL is positioned in the receive path. When JASEL = 0, the JAL is positioned in the transmit path. With JASEL clocked by MCLK, the JAL is disabled. MCLK is the reference for the JAL.

The ES is a 32 x 2-bit register. Data is clocked into the ES with the associated clock signal (TCLK or RCLK), and clocked out of the ES with the dejittered JAL clock. When the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the associated path.

Host Mode provides a dejittered High Frequency Clock (HFC). This 8x clock (12.352 MHz for T1, 16.384 MHz for E1) is tied to the output clock from the JAL. With JA active in the receive path, HFO is tied to RCLK and under LOS conditions defaults to MCLK. With JA active in the transmit path, HFO is tied to TCLK and defaults to MCLK if TCLK is not available. If JA is disabled, HFO is tied to MCLK.

## Built-In Self Test

In Host mode, the LXT332 provides a Built-In Self Test (BIST) mode. Quasi-Random Signal Source (QRSS) generation and detection circuitry is integrated into the LXT332. When the QRSS BIST mode is selected, the LXT332 detects and reports QRSS pattern sync on the incoming signal. When triggered, the LXT332 also transmits the QRSS pattern onto the line. Pattern transmission and detection is independently triggered and reported for each port. Refer to Diagnostic Mode Operation for detailed description.

## Control Modes

The LXT332 transceiver operates in stand alone Hardware (default) Mode or Host Mode depending on the input to the SPE pin. When tied to SPE, MCLK acts as a Serial Port Enable signal to force the LXT332 into its Host mode. The data I/O mode, bipolar or unipolar, is controlled by the TRSTE pin. With TRSTE Low, bipolar I/O is selected. With TRSTE clocked, unipolar I/O is selected. Several diagnostic modes are available on command.

### Host Mode Control

The LXT332 operates in the Host mode when the SPE pin is clocked with MCLK. In Host mode a microprocessor controls the LXT332 through the serial I/O port (SIO) which provides common access to both LIUs. Each of the two LIUs contains a pair of data registers, one for command inputs and one for status outputs. Only one LIU can be selected at a time. If both PS0 and PS1 are active, Port 0 has priority over Port 1. An SIO transaction is initiated by a falling pulse on one of the two Port Select pins, PS0 or PS1. A High-to-Low transition on PS0/1 is required for each subsequent access to the Host mode registers. If both PS0 and PS1 are active simultaneously, Port 0 has priority over Port 1.

The LIU addressed by the PS pulse responds by writing the incoming serial word from the SDI pin into its command register. Figure 4 shows an SIO write operation. The 16-bit serial word consists of an 8-bit Command/Address byte and an 8-bit Data byte. If the command word contains a read request, the addressed LIU subsequently outputs the contents of its status register onto the SDO pin. Figure 5 shows an SIO read operation. The Clock Edge (CLKE) signal determines when the SDO and receive data outputs are valid, relative to the Serial Clock (SCLK) or RCLK as listed in Table 6. Refer to the Test Specifications section for SIO timing.

### Serial Input Word

Figure 4 shows the Serial Input data structure. The LXT332 is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. Bit 1 of the serial Address/Command byte provides Read/Write (R/$\overline{W}$) control when the chip is accessed. The R/$\overline{W}$ bit is set to logic 1 to read the data output byte from the chip, and set to logic 0 to write the input data byte to the chip.

The second 8 bits of a write operation, the Data Input byte, clear Loss of Signal (LOS) and Driver Fail Monitor (DFM) interrupts, reset the chip, and control diagnostic modes. The first 2 bits (D0 – D1) clear and/or mask LOS and DFM interrupts, and the last 3 bits (D5 - D7) control operating

modes (normal and diagnostic) and chip reset. Refer to Table 7 for details on bits D5 – D7 Serial Output Word.

## Serial Output Word

Figure 4 shows the Serial Output data structure. SDO is high impedance when SDI receives an Address/Command byte. If SDI receives a write command (R/W = 0), SDO remains in high impedance. If the command is a read (R/W = 1), then SDO becomes active after the last Command/Address bit (A6) and remains active for eight SCLK cycles. Typically the first bit out of SDO changes the state of SDO from high-z to a Low/High. This occurs approximately 100 µs after the eighth following edge of SCLK.

The output data byte reports Loss of Signal (LOS) and Driver Fail Monitor (DFM) conditions, equalizer settings, and operating modes (normal or diagnostic). The first 5 bits (D0 - D4) report LOS and DFM status, and the Line Length Equalizer settings. The last 3 bits (D5 - D7) report operating modes and interrupt status.

If the $\overline{\text{INT}}x$ line for port *x* is High (no interrupt is pending), bits D5 - D7 report the operating modes listed in Table 8. If the $\overline{\text{INT}}x$ line for port *x* is Low, the interrupt status overrides all other reports and bits D5 - D7 reflect the interrupt status as listed in Table 8.

**Table 6: CLKE Settings**

| CLKE | Output | Clock | Valid Edge |
|---|---|---|---|
| LOW | RPOS/RNEG<br>RDATA<br>SDO | RCLK<br>RCLK<br>SCLK | Rising<br>Rising<br>Falling |
| HIGH | RPOS/RNEG<br>RDATA<br>SDO | RCLK<br>RCLK<br>SCLK | Falling<br>Falling<br>Rising |

**Table 7: SIO Input Bit Settings**
(See Figure 4)

| Mode | RLOOP Bit D5 | LLOOP Bit D6 | TAOS Bit D7 |
|---|---|---|---|
| RLOOP | 1 | 0 | N/A |
| LLOOP | 0 | 1 | N/A |
| DLOOP | 1 | 1 | 1 |
| TAOS | 0 | *n/a* | 1 |
| RESET | 1 | 1 | 0 |

**Table 8: LXT332 Serial Data Output Bit Coding** (See Figure 5)

| Bit | | | Operating Modes |
|---|---|---|---|
| D5 | D6 | D7 | |
| 0 | 0 | 0 | Reset has occurred, or no program input (*i.e.*, normal operation) or DLOOP active.[1] |
| 0 | 0 | 1 | TAOS active |
| 0 | 1 | 0 | LLOOP active |
| 0 | 1 | 1 | TAOS and LLOOP active |
| 1 | 0 | 0 | RLOOP active |
| **Interrupt Status** | | | |
| 1 | 0 | 1 | DFM has changed state since last Clear DFM occured |
| 1 | 1 | 0 | LOS has changed since last Clear LOS occurred |
| 1 | 1 | 1 | DFM and LOS have changed since last Clear DFM and Clear LOS occurred |

1 No explicit status information is available on DLOOP.

**Figure 4: LXT332 SIO Write Operation**

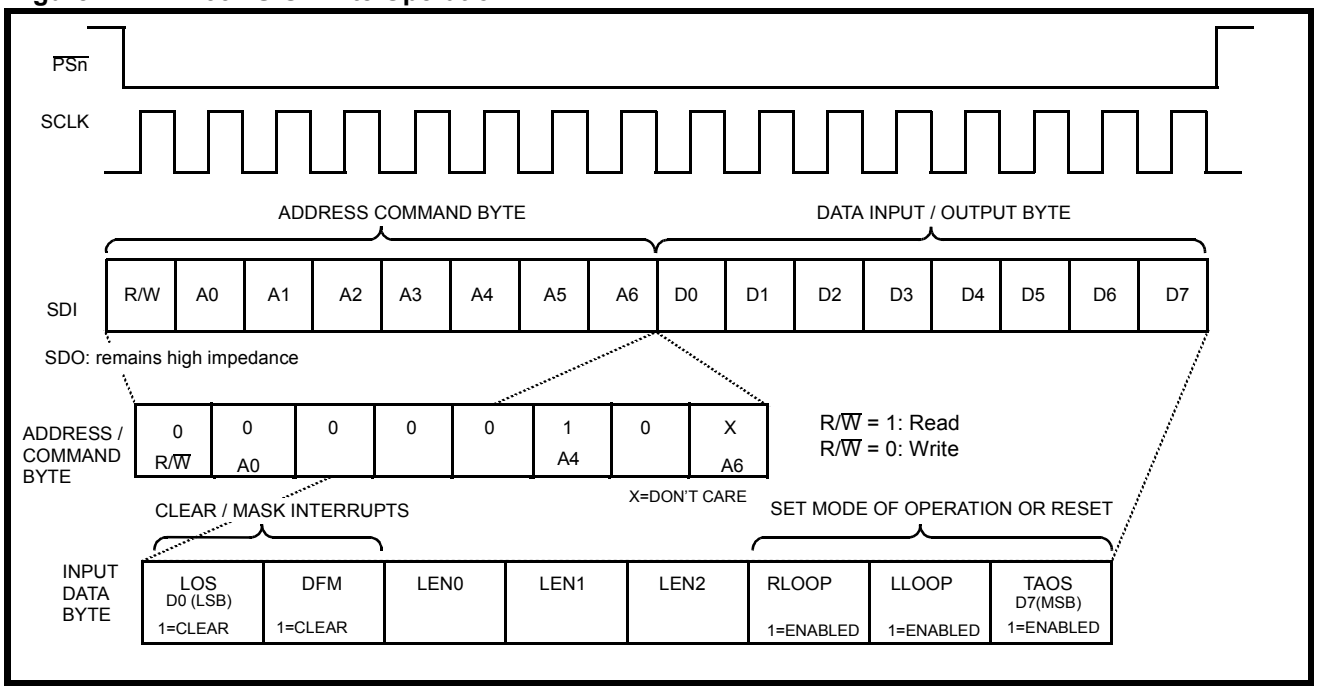
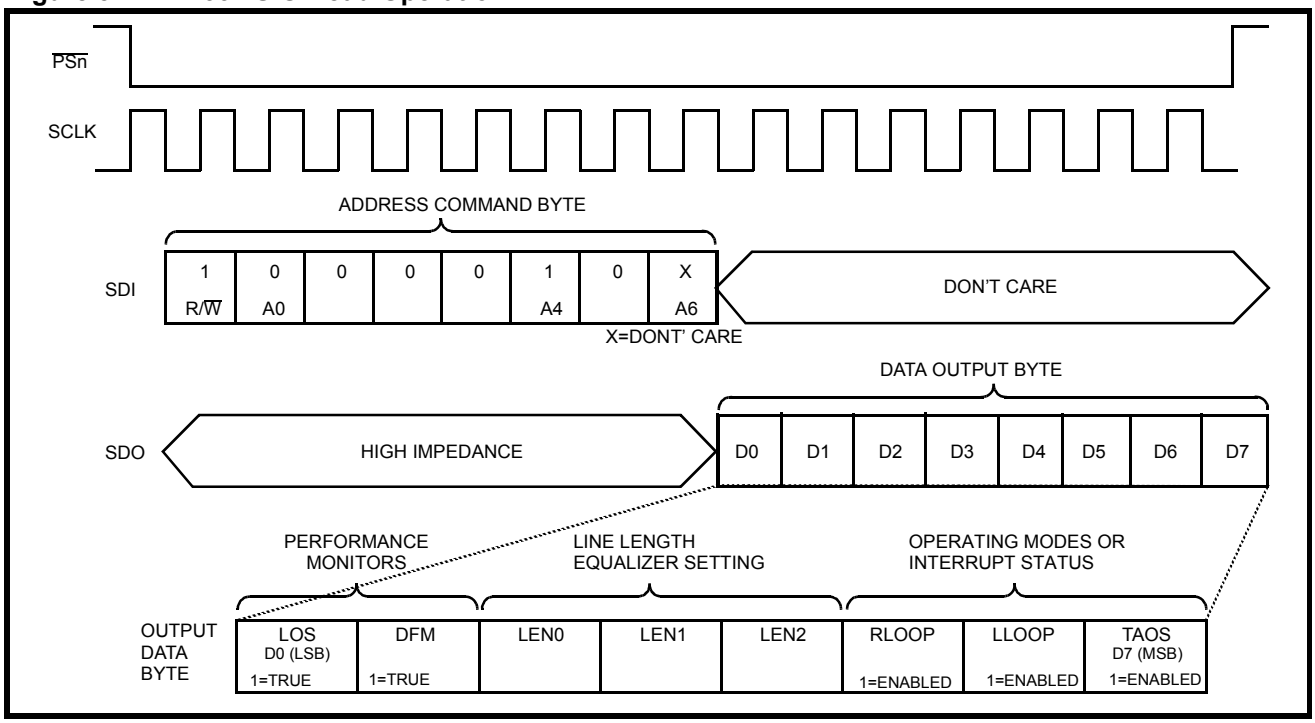



**Figure 5: LXT332 SIO Read Operation**



### Interrupt Handling

The Host mode provides two latched Interrupt output pins, INT0 and INT1, one for each LIU. An interrupt is triggered by a change in the LOS or DFM bits (D0 and D1 of the output data byte, respectively). As shown in Figure 6, either or both interrupt generators can be masked by writing a one to the respective bit of the input data byte (D0 = LOS, D1 = DFM). When an interrupt has occurred, the INTx output pin is pulled Low. The output stage of each INTx pin consists only of a pull-down device. Hence, an external pull-up resistor is required. The interrupt is cleared as follows:

1. If one or both interrupt bits (LOS or DFM, D0 and D1 of the output data byte) =1, writing a 1 to the respective input bit (D0 or D1, respectively, of the input data byte) will clear the interrupt. Leaving a 1 in either of these bit positions will effectively mask the associated interrupt. To re-enable the interrupt capability, reset D0 and/or D1 to 0.
2. If neither LOS or DFM=1, the interrupt will be cleared by resetting the chip. To reset the chip, set data input bits D5 and D6 = 1, and D7 = 0.

## Hardware Mode Control

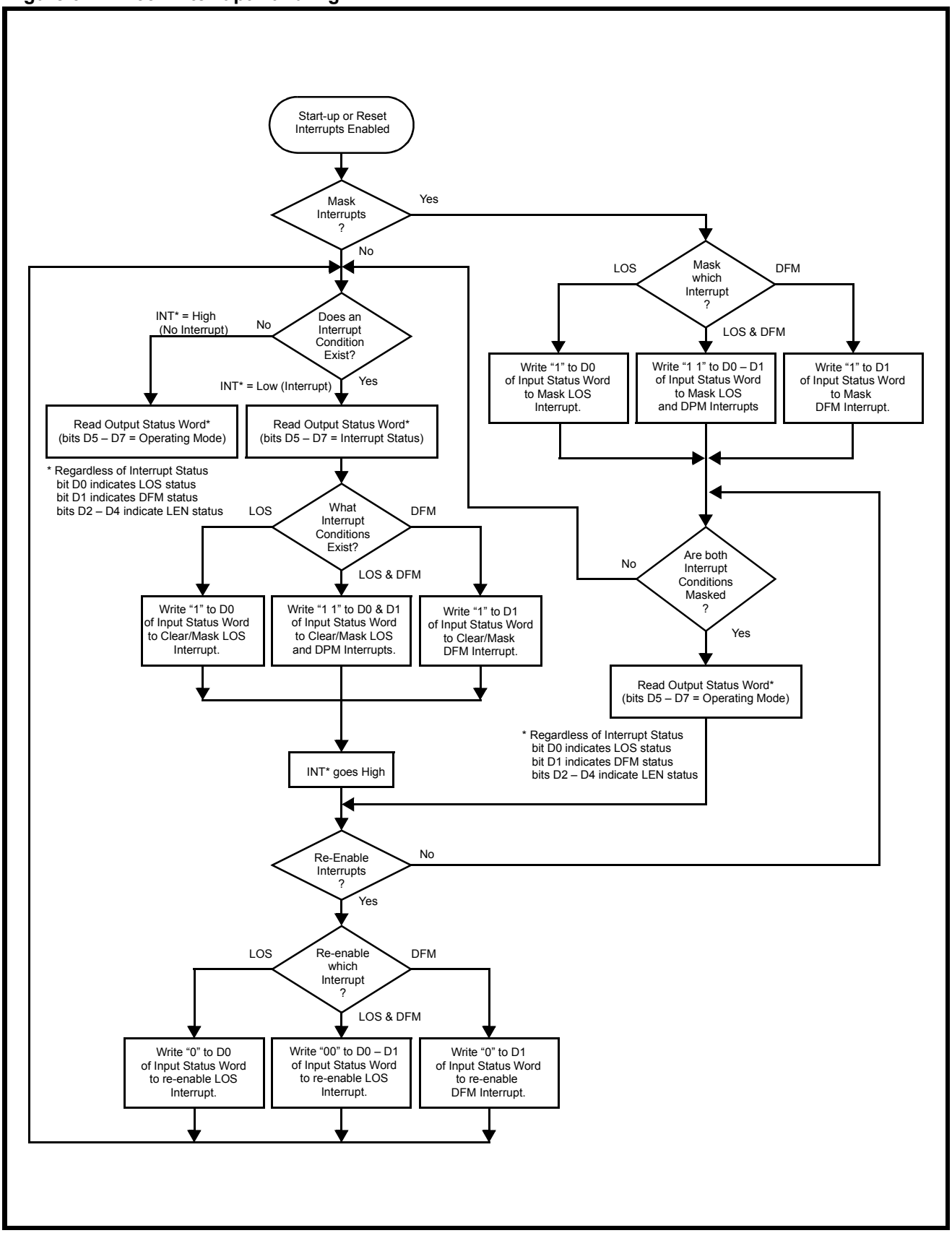
Hardware control is the default operating mode; the LXT332 operates in Hardware mode unless LEN11/SPE pin is clocked. In Hardware mode the transceiver is controlled through individual pins; a µP is not required. The SIO pins are re-mapped to provide control functions. (Data I/O mode selection is unaffected by the control mode. The TRSTE pin selects either unipolar or bipolar data I/O.) In Hardware mode the RPOS/RNEG or RDATA/BPV outputs are valid on the rising edge of RCLK.

## Diagnostic Mode Operation

The LXT332 offers multiple diagnostic modes. Local Loopback (LLOOP), Remote Loopback (RLOOP), Dual Loopback (DLOOP) and Transmit All Ones (TAOS) are available under both Host and Hardware control. An additional Quasi-Random Signal Source (QRSS) mode is available under Host control only.

Under Host control, diagnostic modes are selected by writing the appropriate SIO bits. Under Hardware control, diagnostic modes are selected by a combination of pin settings. The pins must be held at the specified levels for a minimum of 20 ns. The SIO bit names (Host Mode) and pin identifiers (Hardware Mode) for diagnostic functions are identical. Where a particular function can be enabled in either mode, 1=High and 0=Low.

**Figure 6: LX332 Interrupt Handling**



**Transmit All Ones.** See Figure 7. Transmit All Ones (TAOS) is selected when TAOS = 1 and RLOOP = 0. In TAOS mode the TPOS and TNEG inputs are ignored. The TAOS reference clock is determined by setting the jitter attenuator. When jitter attenuation is set for the transmit side, MCLK is used as the reference clock and TCLK is the fall back clock. When JA is set for the receive side, TCLK is the reference clock and MCLK is the fall back clock. When JA is inactive, MCLK is the TAOS reference clock and TCLK is the fall back. TAOS can be commanded simultaneously with Local Loopback as shown in Figure 8, but is inhibited during Remote and Dual Loopback.

**Local Loopback.** See Figures 8 and 9. Local Loopback (LLOOP) is selected when LLOOP = 1 and RLOOP = 0. In LLOOP mode the receiver circuits are inhibited. The transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) are looped back and output at RCLK and RPOS/RNEG or RDATA. During local loopback, the JASEL input functions as follows: If JASEL=0, JA is enabled and active in both the Transmit path and the loopback circuit. If JASEL=1, JA is enabled in the Loopback circuit only. If JASEL = MCLK, JA is disabled.

The transmitter circuits are unaffected by LLOOP. The TPOS/TNEG or TDATA inputs (or a stream of 1s if the TAOS command is active) will be transmitted normally. When used in this mode, the transceiver can be used as a stand-alone jitter attenuator.

**Remote Loopback.** See Figure 10. Remote Loopback (RLOOP) is selected when RLOOP = 1 and LLOOP = 0. (Under this condition, TAOS is ignored. TAOS cannot be commanded simultaneously with RLOOP.) In RLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) are ignored. The RPOS/RNEG or RDATA outputs are looped back to the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the data and clock signals received from the line. During remote loopback, the JASEL input functions as follows: If JASEL = 1, JA is enabled and active in both the Receive path and the loopback circuit. If JASEL = 0, JA is enabled in the Loopback circuit only. If JASEL = MCLK, JA is disabled.

**Dual Loopback.** See Figure 11. Dual Loopback (DLOOP) is selected when RLOOP = 1, LLOOP = 1 and TAOS = 1. In DLOOP mode, the transmit clock and data inputs (TCLK and TPOS/TNEG or TDATA) are looped back through the jitter attenuator (unless disabled by a clock input to the JASEL pin) and output at RCLK and RPOS/RNEG or RDATA. The data and clock recovered from the line are looped back through the transmit circuits and output on TTIP and TRING without jitter attenuation. Unlike the other diagnostic modes, no explicit SIO status indicator is available for DLOOP in the SIO status register.

**Figure 7: TAOS Data Path**

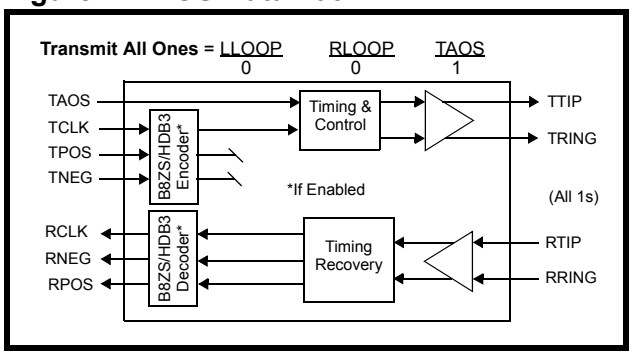



**Figure 8: TAOS with LLOOP & Selectable JA**

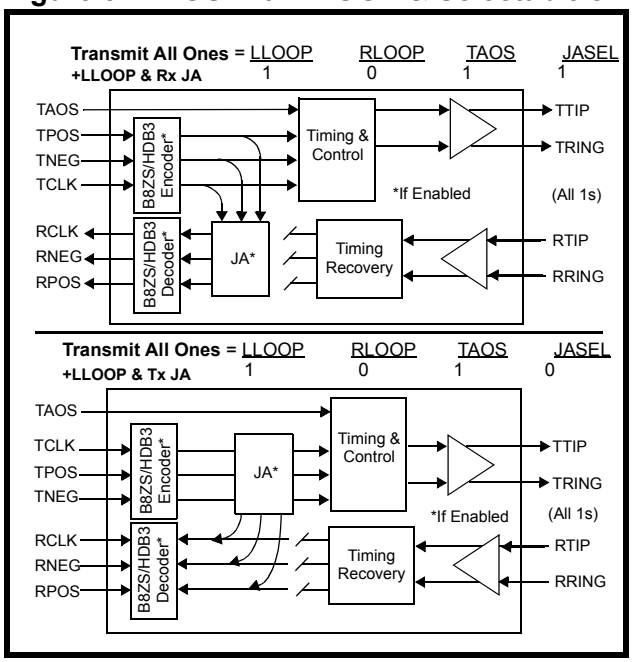
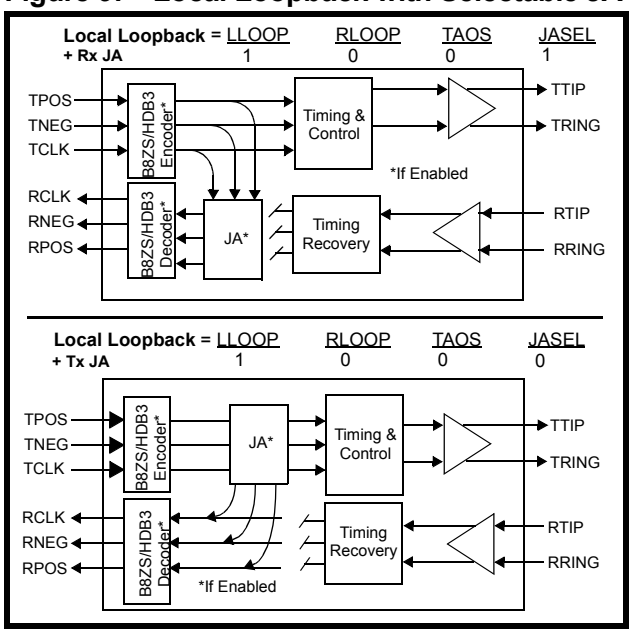



**Figure 9: Local Loopback with Selectable JA**



**QRSS Built-In Self Test (Host Mode only).** See Figure 12. The QRSS Built-In Self Test (BIST) mode is available only under Host control. The QRSS BIST mode is selected by clocking the VCQE pin with MCLK. Once the QRSS BIST mode is selected, the VCQ0 and VCQ1 pins are re-mapped to trigger the QRSS transmission. A High on one of these pins triggers QRSS pattern transmission from the appropriate port. The QRSS pattern for DSX-1 systems is $2^{20}$-1, with no more than 14 consecutive zeros. For CEPT systems the QRSS pattern is $2^{15}$-1. The QRSS pattern is locked to MCLK. Once the QRSS transmission is activated, errors can be inserted into the transmit data stream by causing a Low-to-High transition on the TPOS/TDATA pin for the respective port. In Bipolar mode, Low-High transitions cause both a logic error and a bipolar violation to be inserted into the QRSS data stream. In Unipolar mode, only a logic error is inserted.

The Pattern Detect circuitry is activated by the QRSS BIST mode, although the basic receive circuits are unaffected. The Pattern Detect (PD*n*) pins indicate QRSS pattern sync. The Pattern Detect pin stays High until synchronization is achieved on the QRSS pattern. The QRSS pattern is considered in sync when there are fewer than 4 errors in 128 bits. The PD pin goes High indicating an out-of-sync conditions if 4 or more errors are detected in 128 bits (i.e. sync is defined as fewer than 4 errors in 128 bits).

## Initialization/Reset Operation

Upon initial power up, the transceiver is held static until the power supply reaches approximately 3 V. Upon crossing this threshold, the device clears all internal registers and begins calibration of the delay lines. A reference clock is required to calibrate the delay lines. TCLK is the transmit reference, and MCLK is the receive reference. The PLLs are continuously calibrated.

The transceiver can be reset from the Host or H/W mode. In Host mode, reset is commanded by writing 1s to RLOOP and LLOOP, and a 0 to TAOS (bits D5, D6 and D7, respectively, of the SIO input data byte). In H/W mode, reset is commanded by simultaneously holding RLOOP and LLOOP High, and TAOS Low, for approximately 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, each port is reset independently. Reset clears and sets all SIO registers to 0 at the affected port. Reset is not generally required for the port to be operational.

**Figure 10: Remote Loopback with Selectable JA**

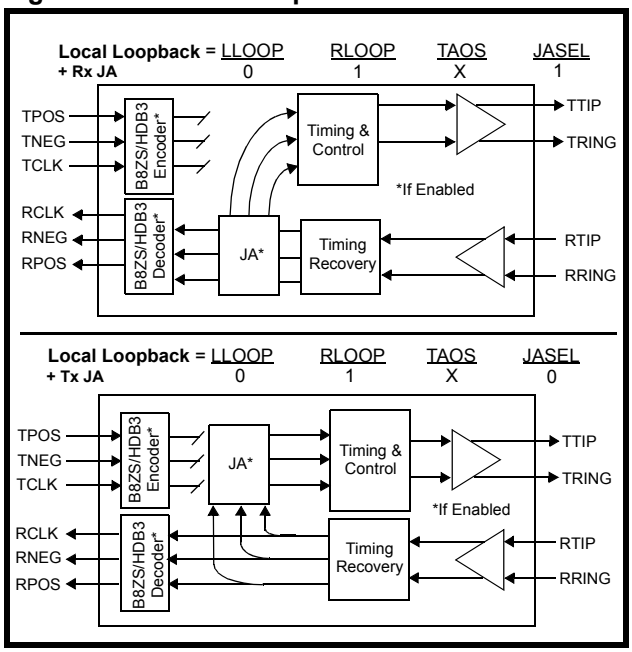



**Figure 11: Dual Loopback**

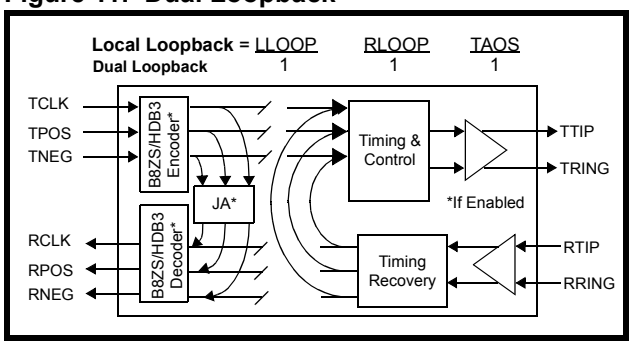
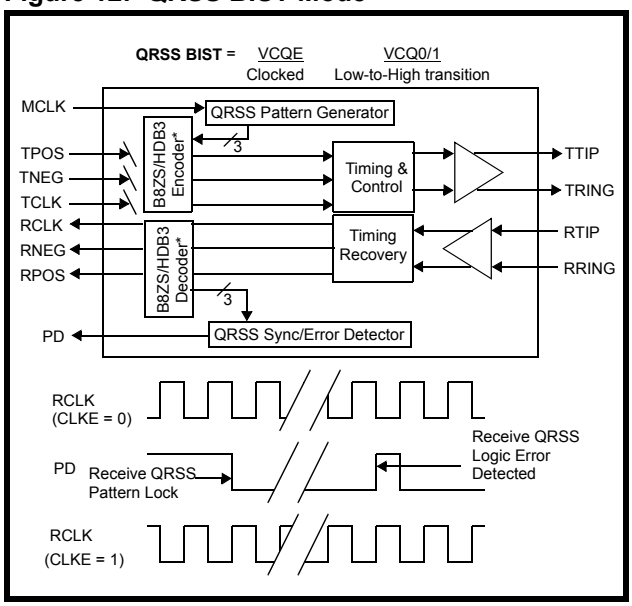



**Figure 12: QRSS BIST Mode**



# APPLICATION INFORMATION

## Power Requirements

The LXT332 is a low-power CMOS device. It operates from a single +5 V power supply which can be tied to all three VCC inputs. However, all inputs must be within ± .3 V of each other, and decoupled to their respective grounds separately. Isolation between the transmit and receive circuits is provided internally. During normal operation or local loopback, the transmitter powers down if TCLK is not supplied.

## Transformers

The transformer specifications listed in Table 9 give the correct impedance matching for balanced transmit or receive lines. Table 10 shows the combinations of resistors and transformers to produce a variety of return loss values depending on the LEN code settings chosen for a specific design

## 1.544 Mbps T1 Applications

Figure 13 shows a typical host mode application. The eight serial interface pins are grouped at the top. Host mode is selected by the clock input to SPE. Other mode selection pins are shown at the bottom. With the TRSTE pin switched Low, the LXT332 operates in the bipolar I/O mode. Driving JASEL Low switches the jitter attenuation circuits into the transmit paths for both LIU ports.

Figure 13 shows a pair of framers (a dual framer could also be used). A LXP600A Clock Adapter (CLAD) converts the 2.048 MHz backplane clock to provide the 1.544 MHz input to the MCLK and TCLK inputs of both LIU ports.

The DFM and PD indicators and High frequency clocks are grouped in the diagram lower left. These outputs are available to drive optional external circuits. The driver power supply inputs (lower right) are tied to a common bus with 1.0 µF decoupling capacitors installed. The power supply for the remaining (non-driver) circuitry is shown at center right with 68 µF and 0.1 µF decoupling capacitors.

The line interface circuitry is identical for both LIU ports. The precision resistors in line with the transmit transformer provide optimal return loss. The recommended transformer/resistor combinations are listed at the bottom of Figure 15. Center tapped 2:1 transformers are used on the receive side.

**Table 9: Recommended Transformer Values**

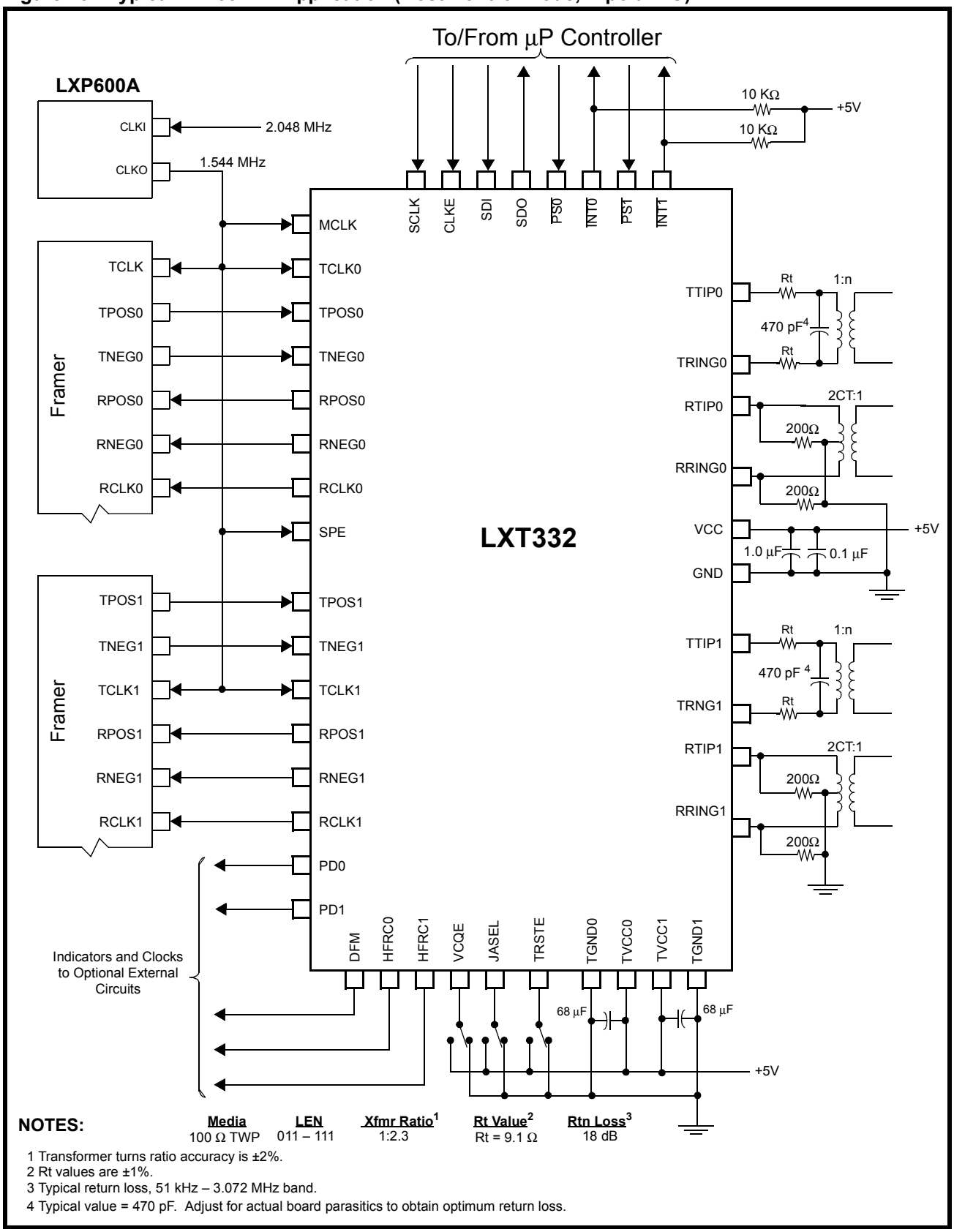
| Parameter | Value |
|---|---|
| Turns Ratio (T1) | 1:2.3 (Tx) / 1:2 CT (Rx) |
| Turns Ratio (E1) | 1:2 (Tx) / 1:2 CT (Rx) |
| Primary Inductance | 1.2 mH maximum |
| Leakage Inductance | 0.5 µH maximum |
| Interwinding Capacitance | 25 pF maximum |
| DC Resistance (Pri.) | 1 Ω maximum |
| ET (Breakdown Voltage) | 1 kV minimum |

**Table 10: Transformer Combinations**

| LEN | Xfmr Ratio[1] | Rt Value[2] | Rtn Loss[3] |
|---|---|---|---|
| **For T1/DSX-1 100 Ω Twisted-Pair Applications:** | | | |
| 011 – 111 | 1:2 | Rt = 9.1 Ω | 14 dB |
| 011 – 111 | 1:2.3 | Rt = 9.1 Ω | 18 dB |
| 011 – 111 | 1:1.15 | Rt = 0 Ω | 18 dB |
| **For E1 120 Ω Twisted-Pair Applications:** | | | |
| 001 | 1:2 | Rt = 15 Ω | 18 dB |
| 000 | 1:2 | Rt = 9.1 Ω | 10 dB |
| **For E1 75 Ω Coaxial Applications:** | | | |
| 001 | 1:2 | Rt = 14.3 Ω | 10 dB |
| 000 | 1:2 | Rt = 9.1 Ω | 18 dB |

1 Transformer turns ratio accuracy is ±2 %.
2. Rt values are ±1 %.
3. Typical return loss, 51 kHz – 3.072 MHz, with a capacitor in parallel with the primary side of the transformer.

**Figure 13: Typical LXT332 T1 Application (Host Control Mode, Bipolar I/O)**



# 2.048 Mbps E1/CEPT Interface Applications

## E1 Coaxial Applications

Figure 14 shows the line interface for a typical 2.048 Mbps E1 coaxial (75Ω) application. The LEN code should be set to 000 for coax. With 9.1Ω Rt resistors in line with the 1:2 output transformers, the LXT332 produces 2.37 V peak pulses as required for coax applications. As in the T1 application shown in Figure 13, center tapped 1:2 transformers are used on the receive side.

## E1 Twisted-Pair Applications

Figure 15 shows a typical 2.048 Mbps E1 twisted-pair (120Ω) application. With the TRSTE pin tied to ground the LXT332 operates in the bipolar data I/O mode. The JA circuit is placed in the transmit path by the Low on JASEL The line length equalizers are controlled by the hardwired LEN inputs. With the LEN code set to 001 and 15Ω Rt resistors in line with the 1:2 output transformers, the LXT332 produces the 3.0 V peak pulses required for this application. Center tapped 1:2 transformers are used on the receive side.

A single clock source provides the 2.048 MHz input to MCLK and TCLK. The DFM pin may routed to an LED driver or other indicator, or be left unconnected. Switches on the TAOS, LLOOP and RLOOP inputs provide mode control and hardware reset capability.

As in Figure 15, the power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

**Figure 14: Line Interface for E1 Coax Applications**

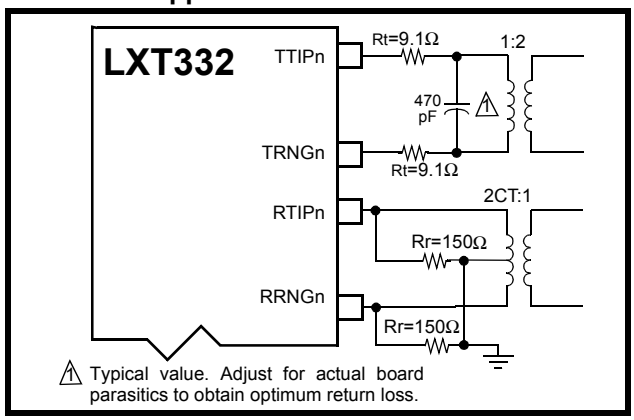
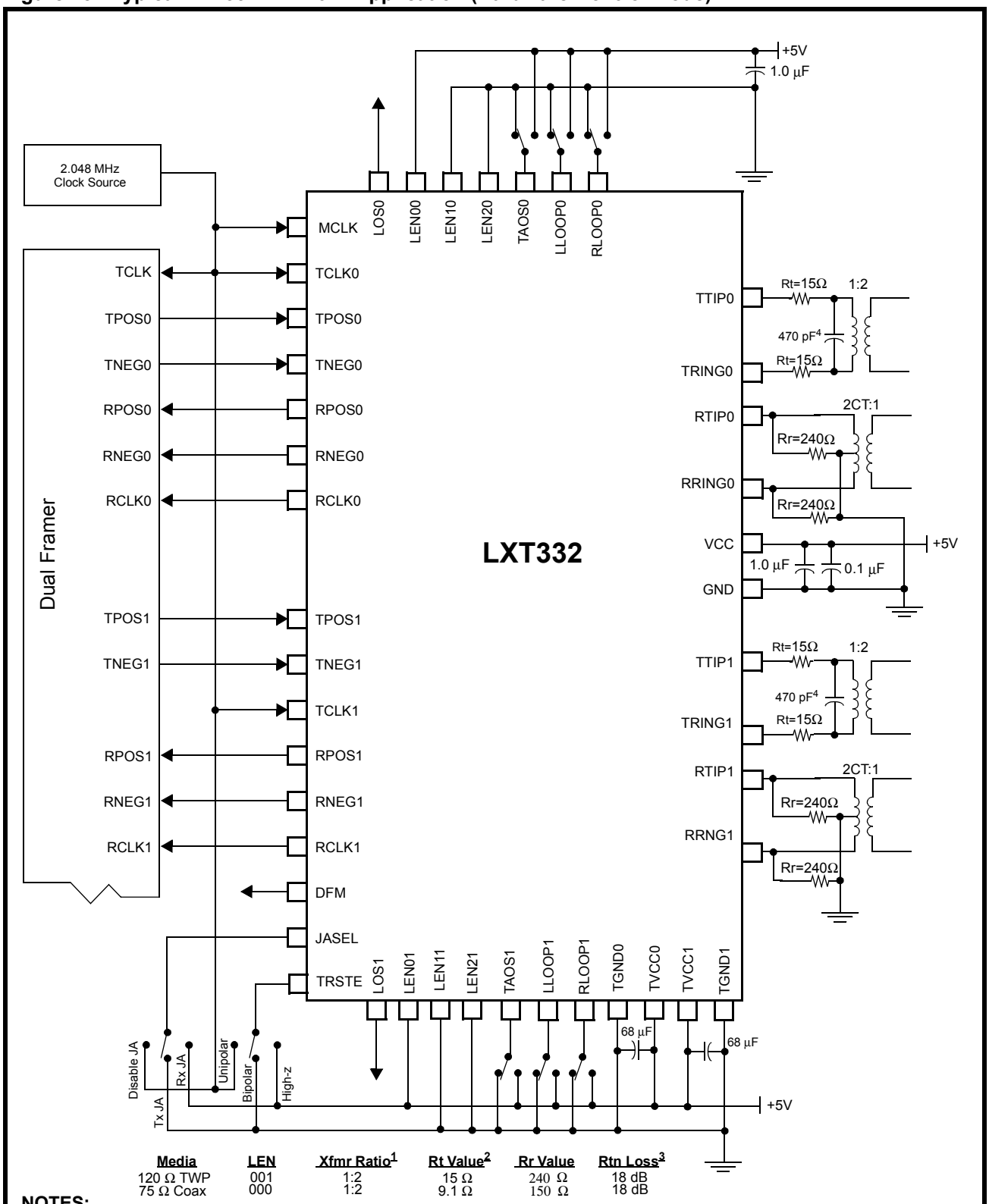


**Figure 15: Typical LXT332 E1 120 Ω Application (Hardware Control Mode)**




**NOTES:**

1 Transformer turns ratio accuracy is ±2%.
2 Rt values are ±1%.
3 Typical return loss, 51 kHz – 3.072 MHz band.
4 Typical value = 470 pF. Adjust for actual board parasitics to obtain optimum return loss.

# TEST SPECIFICATIONS

**NOTE**

Information in Tables 11 through 17 and Figures 16 through 21 represent the performance specifications of the LXT332 Dual Line Interface Unit and are guaranteed by test, except as noted, by design.

**Table 11: Absolute Maximum Ratings**

| Parameter | Sym | Min | Max | Units |
|---|---|---|---|---|
| DC supply (referenced to GND) | VCC, TVCC0, TVCC1 | – | 6.0 | V |
| Input voltage, any pin [1] | $V_{IN}$ | GND - 0.3 | $V_{CC}$ + 0.3 | V |
| Input current, any pin [2] | $I_{IN}$ | -10 | 10 | mA |
| Storage temperature | $T_{STG}$ | -65 | +150 | °C |

**CAUTION**

Operations at or beyond these limits may result in damage to the device.
Normal operation not guaranteed at these extremes.

1 Excluding RTIP and RRING which must stay between -6 V and $V_{CC}$ + 0.3 V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+, and TGND can withstand continuous current of 100 mA.

**Table 12: Recommended Operating Conditions**

| Parameter | Symbol | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| DC supply [1] | VCC, TVCC0, TVCC1 | 4.75 | 5.0 | 5.25 | V |
| Ambient operating temperature | $T_A$ | -40 | 25 | 85 | °C |

1 Variation between TVCC0, TVCC1 and VCC must be within ±0.3 V of each other during steady state and transient conditions.

**Table 13: Electrical Characteristics** (Over Recommended Range)

| Parameter | Sym | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Total power dissipation – T1 [1] (Maximum line length) | $P_D$ | – | 700 | 900 | mW | 100% ones density |
| | $P_D$ | – | 550 | 700 | mW | 50% ones density |
| Total power dissipation – E1 [1] | $P_D$ | – | 575 | 700 | mW | 100% ones density |
| | $P_D$ | – | 490 | 600 | mW | 50% ones density |
| High level input voltage [2,3] | $V_{IH}$ | 2.0 | – | – | V | |
| Low level input voltage [2,3] | $V_{IL}$ | – | – | 0.8 | V | |
| High level output voltage [2,3] | $V_{OH}$ | 2.4 | – | – | V | $I_{OUT}$ = -400 µA |
| Low level output voltage [2,3] | $V_{OL}$ | – | – | 0.4 | V | $I_{OUT}$ = 1.6 mA |
| Input leakage current [4] | $I_{LL}$ | 0 | – | ±10 | µA | |
| Three-state leakage current [2] | $I_{SL}$ | 0 | – | ±10 | µA | |
| Input pull down current (MCLK)[5] | | | – | 100 | µA | |
| TTIP/TRING leakage current | $I_{TR}$ | – | – | 1.2 | mA | In tri-state and power down modes |

1 Total power dissipation includes the device power consumption and load power dissipation while driving a 75 Ω load on the secondary side. The T1 test circuit is a 100 Ω line load connected to the driver outputs via a 1:1.15 turns ratio transformer without series resistors.
2. Functionality of pins depends on mode.
3. Output drivers will output CMOS logic levels into CMOS loads.
4. Except for MCLK, RTIP0, RRING0, RTIP1, and RRING1.
5. Applies to pins 8,11,23,26

**Table 14: Analog Specifications** (Over Recommended Range)

| Parameter | | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| AMI Output Pulse Amplitudes | DSX-1 | 2.4 | 3.0 | 3.6 | V | measured at the DSX |
| | E1 (120 Ω) | 2.7 | 3.0 | 3.3 | V | measured at line side |
| | E1 (75 Ω) | 2.13 | 2.37 | 2.61 | V | measured at line side |
| Transmit amplitude variation with supply [3] | | – | 1 | 2.5 | % | |
| Recommended output load at TTIP and RRING | | – | 75 | – | Ω | |
| Driver output impedance [3] | | – | 3 | 10 | Ω | @ 772 kHz |
| Jitter added by the transmitter [1] | 10 Hz - 8 kHz [3] | – | 0.005 | 0.01 | UI | T1 Jitter based |
| | 8 kHz - 40 kHz [3] | – | 0.015 | 0.025 | UI | |
| | 10 Hz - 40 kHz [3] | – | 0.02 | 0.025 | UI | |
| | Broad Band | – | 0.03 | 0.05 | UI | |
| Jitter added by the transmitter [1] | 20 Hz – 100 kHz | – | – | 0.05 | UI | E1 Jitter Band |
| Output power levels [3] | @772 kHz | 12.6 | – | 17.9 | dBm | |
| DS1 2 kHz BW | @ 1544 kHz | -29 | – | – | dB | referenced to power in 2 kHz band at 772 kHz |
| Positive to negative pulse imbalance | | – | – | 0.5 | dB | |
| Receive input impedance | | – | 40 | – | kΩ | |
| Sensitivity below DSX | (0 dB = 2.4 V) | 13.6 | – | – | dB | |
| (max 6 dB cable attenuation) | | 500 | – | – | mV | |
| Loss of Signal threshold | | – | 0.3 | – | V | |
| Data decision threshold | DSX-1 | 60 | 70 | 77 | % peak | |
| | E1 | 43 | 50 | 57 | % peak | |
| Input jitter tolerance | 10 Hz | – | 1200 | – | UI | |
| | 750 Hz | 14 | – | – | UI | |
| | 10 kHz – 100 kHz | 0.4 | – | – | UI | |
| Allowable consecutive zeros before LOS | | 160 | 175 | 190 | – | |
| Jitter attenuation curve corner frequency [2,3] | T1 | – | 6 | – | Hz | |
| | E1 | – | 10 | – | Hz | |
| Attenuation input jitter tolerance before FIFO overflow [3] | | 28 | – | – | UI | |
| Jitter attenuation @ 10 kHz | | | 45 | – | dB | |

1 Input signal to TCLK is jitter-free.
2. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
3. Not production tested, but guaranteed by design and other correlation models.

**Table 15: LXT332 Serial I/O Timing Characteristics** (See Figures 16 and 17)

| Parameter | Sym | Min | Typ[1] | Max | Units | |
|---|---|---|---|---|---|---|
| Rise/Fall time - any digital output | $t_{RF}$ | – | – | 100 | ns | Load 1.6 mA, 50 pF |
| SDI to SCLK setup time | tDC | 50 | – | – | ns | |
| SCLK to SDI hold time | $t_{CDH}$ | 50 | – | – | ns | |
| SCLK Low time | $t_{CL}$ | 240 | – | – | ns | |
| SCLK High time | $t_{CH}$ | 240 | – | – | ns | |
| SCLK rise and fall time | $t_R$, $t_F$ | – | – | 50 | ns | |
| PS to SCLK setup time | $t_{PC}$ | 50 | – | – | ns | |
| SCLK to PS hold time | $t_{CPH}$ | 50 | – | – | ns | |
| PS inactive time | $t_{PWH}$ | 250 | – | – | ns | |
| SCLK to SDO valid | $t_{CDV}$ | – | – | 200 | ns | |
| SCLK falling edge or PS rising edge to SDO high-z | $t_{CDZ}$ | – | 100 | – | ns | |

1 Typical figures are at 25 °C and are design aid only; not guaranteed and not subject to production testing.

**Figure 16: LXT332 Serial Data Input Timing Diagram**

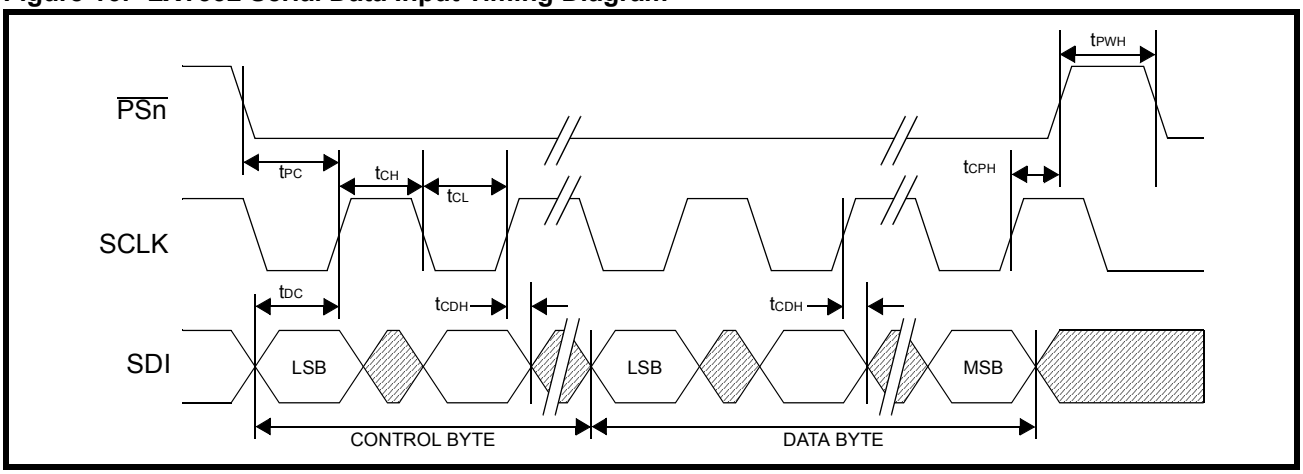


**Figure 17: LXT332 Serial Data Output Timing Diagram**

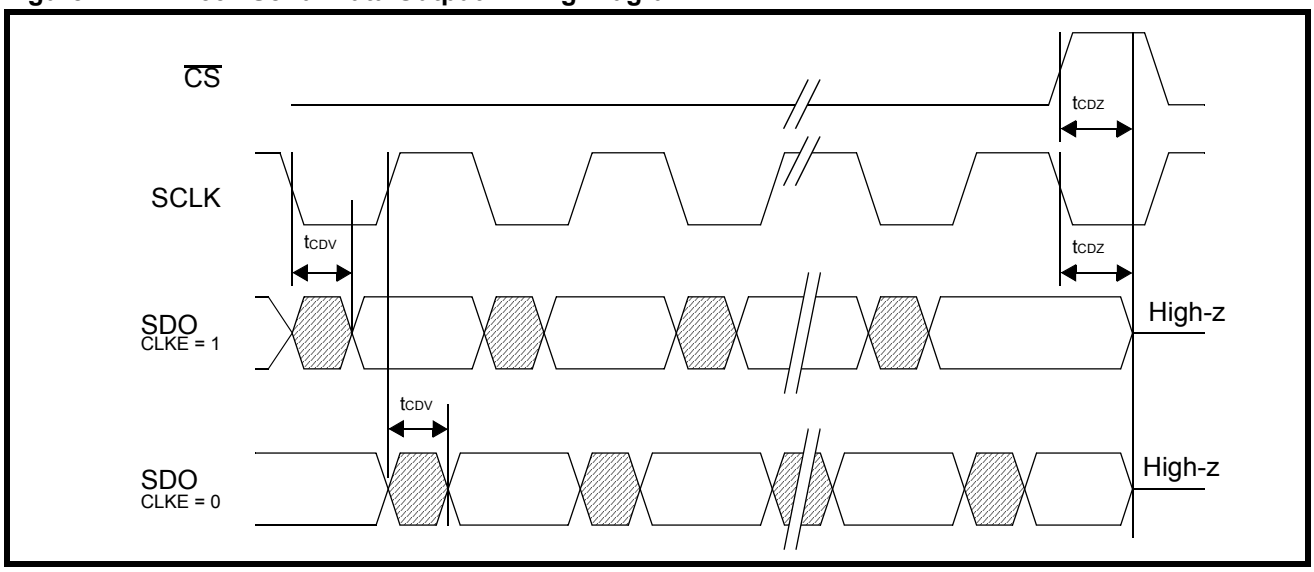



**Figure 18: LXT332 Receive Clock Timing**

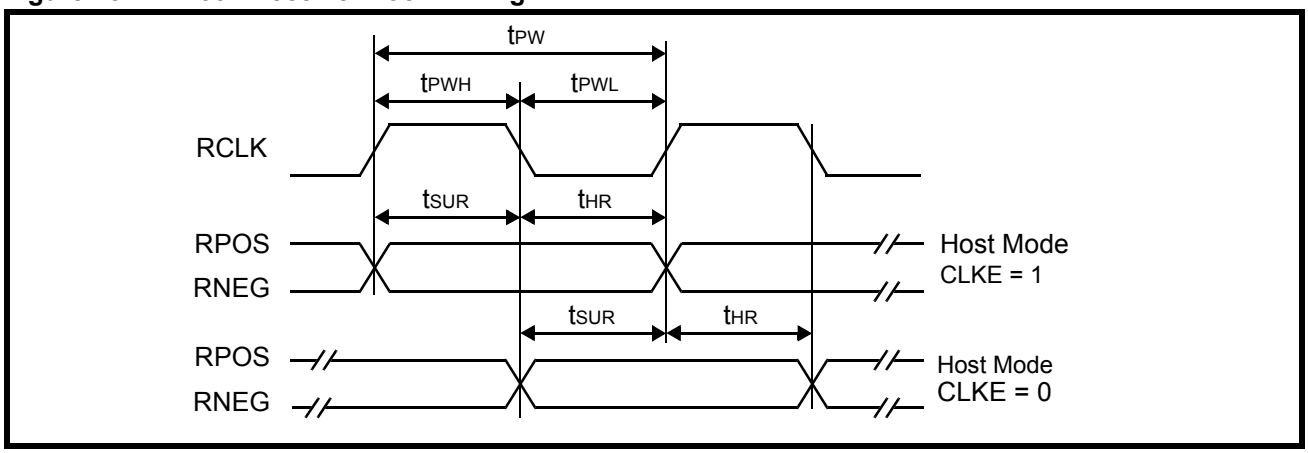



**Figure 19: LXT332 Transmit Clock Timing**

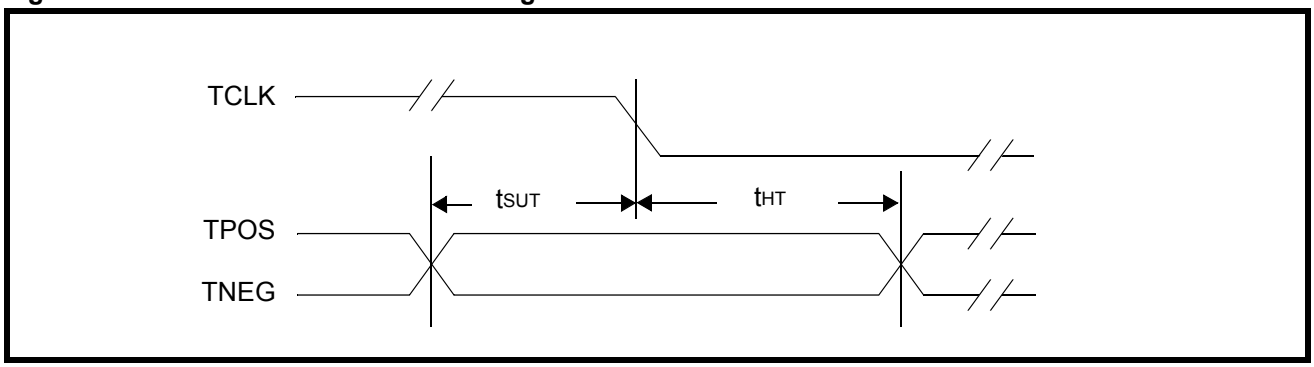


**Table 16: LXT332 Receive Timing Characteristics** (See Figure 18)

| Parameter | | Sym | Min | Typ[1] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| Receive clock period | DSX-1 | $t_{PW}$ | 583 | 648 | 713 | ns | Elastic store not in overflow or underflow. |
| | E1 | $t_{PW}$ | 439 | 488 | 537 | ns | |
| Receive clock duty cycle | | RCLKd | 40 | 50 | 60 | ns | |
| Receive clock pulse width High | DSX-1 | $t_{PWH}$ | 259 | 324 | 389 | ns | |
| | E1 | $t_{PWH}$ | 195 | 244 | 293 | ns | |
| Receive clock pulse width Low | DSX-1 | $t_{PWL}$ | 259 | 324 | 389 | ns | |
| | E1 | $t_{PWL}$ | 195 | 244 | 293 | ns | |
| RPOS / RNEG to RCLK rising setup time | DSX-1 | $t_{SUR}$ | 50 | 274 | – | ns | |
| | E1 | $t_{SUR}$ | 50 | 194 | – | ns | |
| RCLK rising to RPOS / RNEG hold time | DSX-1 | $t_{HR}$ | 50 | 274 | – | ns | |
| | E1 | $t_{HR}$ | 50 | 194 | – | ns | |

1 Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

**Table 17: LXT332 Master Clock and Transmit Timing Characteristics** (See Figure 19)

| Parameter | | Sym | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| Master clock frequency | DSX-1 | MCLK | – | 1.544 | – | MHz |
| | E1 | MCLK | – | 2.048 | – | MHz |
| Master clock tolerance | | MCLKt | – | ±50 | – | ppm |
| Master clock duty cycle | | MCLKd | 40 | – | 60 | % |
| Transmit clock frequency | DSX-1 | TCLK | – | 1.544 | – | MHz |
| | E1 | TCLK | – | 2.048 | – | MHz |
| Transmit clock tolerance | | TCLKt | – | ±50 | – | ppm |
| Transmit clock duty cycle | | TCLKd | 10 | – | 90 | % |
| TPOS/TNEG to TCLK setup time | | $t_{SUT}$ | 50 | – | – | ns |
| TCLK to TPOS/TNEG Hold time | | $t_{HT}$ | 50 | – | – | ns |

1 Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

**Figure 20: Typical Receiver Input Jitter Tolerance (Loop Mode)**

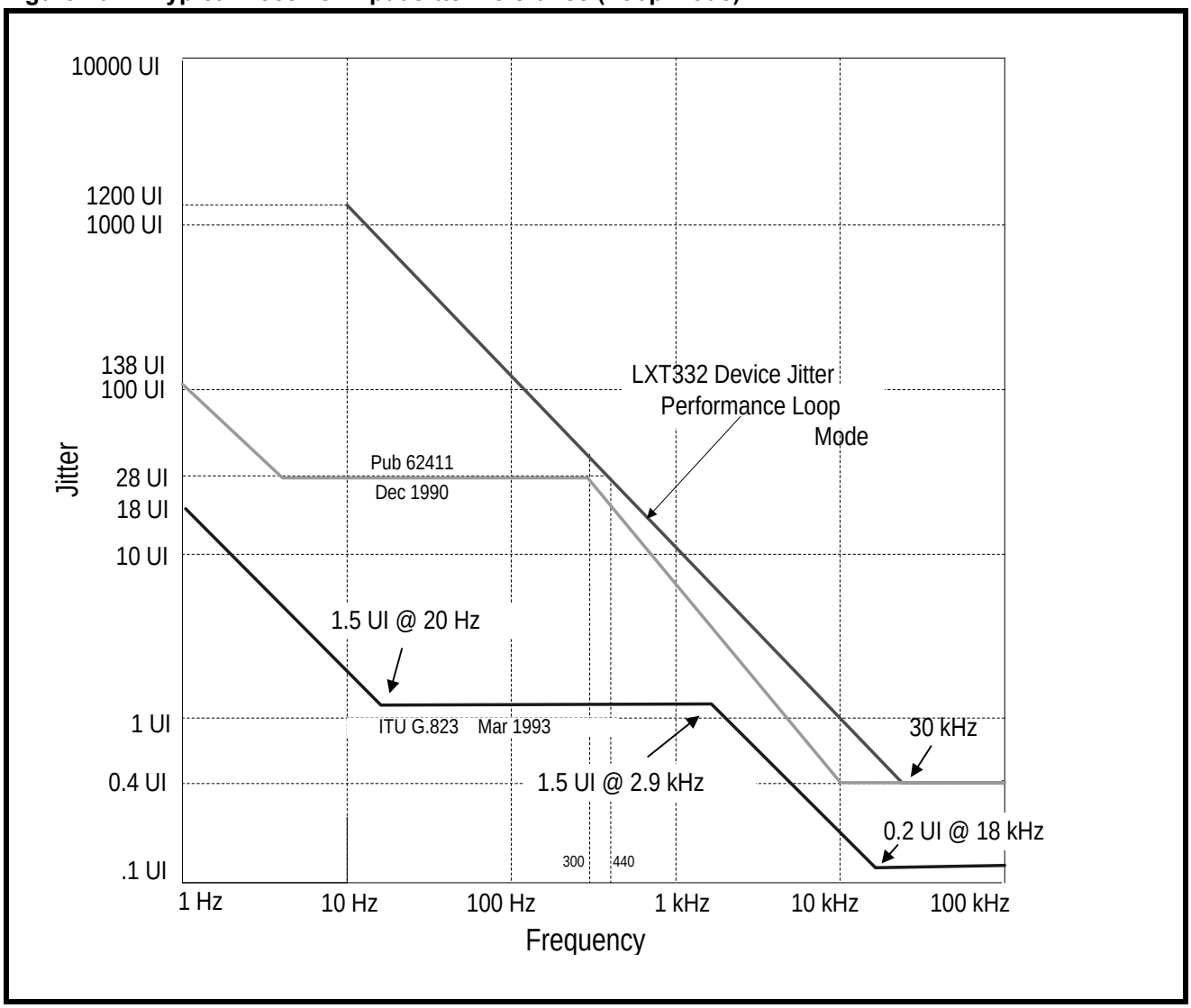
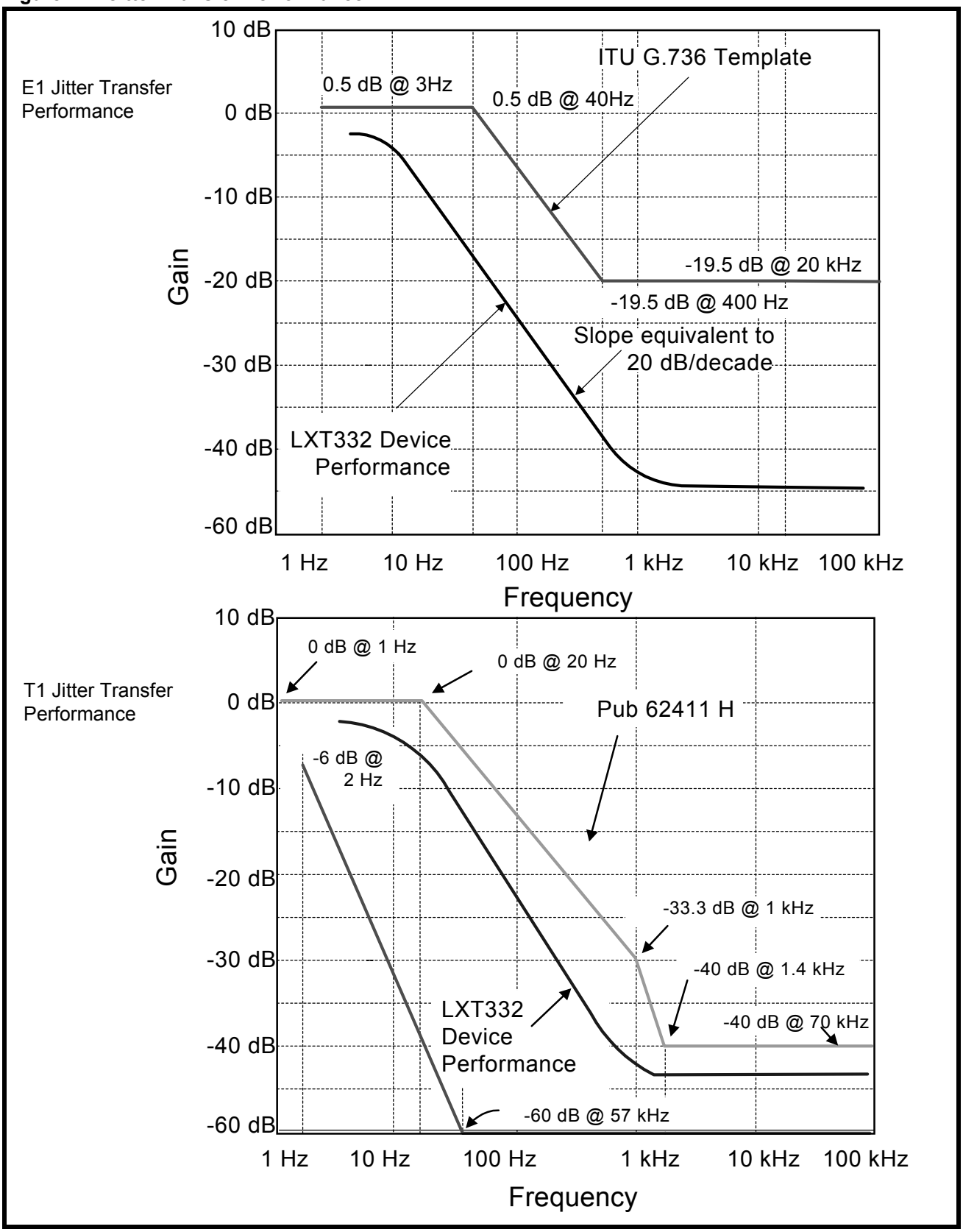


**Figure 21: Jitter Transfer Performance**



# APPENDIX A

## Data Sheet Changes

The following table lists changes that have been made to the February 1997 printing of the LXT332 data sheet. The previous version of the data sheet is dated May 1996.

| Page Number | Section/Figure/Table | Change Made |
|---|---|---|
| 12 | Functional Description, Receiver subhead | For T1 applications, changed to say LEN does not equal 000 to 001 |
| 14 | Functional Description, Driver Failure Monitor subhead | Removed sentences pertaining to the assertion of an interrupt line in host mode—already covered in the "Interrupt Handling" section on page 17. |
| 19 | Functional Description, Transmit All Ones subsection | Information added about how jitter attenuator affects TAOS reference clock. |
| 20 | Figure 10: Remote Loopback with Selectable JA | In second figure, changed JASEL from 1 to 0 |
| 24 | Figure 15: Typical 120 Ω Application (Hardware Mode) | Swapped High Z and Unipolar switches at the bottom left corner of the figure |
| 26 | Table 14: Analog Specifications | The Typical value of data decision threshold for DSX-1 was changed from 50 to 70 % peak. |
| 28 | Figure 18: LXT332 Receive Clock Timing | New figure |
| 29 | Table 17: Master Clock and Transmit Timing Characteristics | Minimum values for TCLK setup and hold times (last two rows) changed from 25 ns to 50 ns |