

■ OVERVIEW

The SM5619 series is a range of quartz crystal oscillator ICs fabricated using NPC's original molybdenum-gate CMOS technology. Each IC consists of a low-current oscillator circuit and output buffer. With master slice, the output level can be selected between TTL and CMOS, and the output current between 16 mA and 4 mA. The IC also incorporates a high-precision, thin-film feedback resistor and oscillation capacitors having excellent frequency characteristics.

■ FEATURES

- Up to 30 MHz
- Fundamental wave
- Built-in feedback resistor in inverter amplifier
- Built-in loading capacitors CG and CD
- Output tristate function
- Low quartz current
- Chip form
- Input TTL compatible
- Operating voltage 4.5 to 5.5 V
- Low current consumption
- Chip form
- Molybdenum-gate® CMOS construction

■ PIN DESCRIPTION

Name	Function
XT	Oscillation input
XT	Oscillation output
INH	"L": output high impedance. Internal pull-up resistor.
V _{DD}	Supply voltage
V _{SS}	Ground
Q	Output (One of fo, fo/2, fo/4 and fo/8 is output according to internal wiring.)

■ SERIES LINEUP

Version	Output frequency	Output duty level	Output current (mA)
SM5619 N1	fo	CMOS	16
N3	fo/2	CMOS	16
N5	fo/4	CMOS	16
N7	fo/8	CMOS	16
H1	fo	CMOS	4
H3	fo/2	CMOS	4
H5	fo/4	CMOS	4
H7	fo/8	CMOS	4
K1	fo	TTL	16

■ BLOCK DIAGRAM

■ FUNCTIONAL DESCRIPTION

Control pin	Output pin
INH	Q
H (open)	One of fo, fo/2, fo/4 and fo/8
L	High impedance

fo: fundamental frequency

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Item	Symbol	Rating		Unit
Supply voltage	V _{DD}	-0.5 to +7.0		V
Input voltage	V _{IN}	-0.5 to V _{DD} +0.5		V
Output voltage	V _{OUT}	-0.5 to V _{DD} +0.5		V
Storage temperature	T _{STG}	-65 to +150		°C
Output current	I _{OUT}	H series N series K1 servion	10 25	mA

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Item	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V _{DD}	4.5	5.0	5.5	V
Input voltage	V _{IN}	V _{SS}		V _{DD}	V
Operating temperature	T _{OPR}	-20		+80	°C

■ ELECTRICAL CHARACTERISTICS

1. N series, K1 version (V_{DD} = 5 ± 0.5 V, V_{SS} = 0 V and Ta = -20 to +80°C unless otherwise specified)

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
H-level output voltage	V _{OH}	Q pin, Fig. 1	V _{DD} =4.5V, I _{OH} =16.0mA	3.9	4.2		V
L-level output voltage	V _{OL}		V _{DD} =4.5V, I _{OL} =16.0mA		0.3	0.4	
Output leak current	I _Z	Q pin, Fig. 1, INH pin="L", V _{DD} =5.5V	V _{OH} =V _{DD} , V _{OL} =V _{SS}			10	μA
H-level input voltage	V _{IH}	INH pin		2.0			
L-level input voltage	V _{IL}					0.8	
Current consumption	I _{DD1}	Load circuit 1, Fig. 2, Cl=15pF, INH=OPEN, f=30MHz	SM5619N1	C _L =15pF	13	23	mA
				C _L =50pF	18	32	
			SM5619N3	C _L =15pF	9	16	
				C _L =50pF	12	21	
			SM5619N5	C _L =15pF	7	13	
				C _L =50pF	9	16	
			SM5619N7	C _L =15pF	6	11	
				C _L =50pF	7	13	
			SM5619K1	C _L =15pF	13	23	
Pull-up resistor	R _{UP}	INH pin, Fig. 3		50		250	kΩ
Feedback resistor	R _f	Fig. 4		90	100	110	kΩ
Inverter amplifier output resistor	R _D	Calculated from R _f		740	820	900	Ω
Internal capacitor	C _G			18.9	21	23.1	pF
	C _D			18.9	21	23.1	

2. H series

(V_{DD} = 5 ± 0.5 V, V_{SS} = 0 V and Ta = -20 to +80°C unless otherwise specified)

ITEM	SYMBOL	CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
H-level output voltage	V _{OH}	Q pin, Fig. 1	V _{DD} =4.5V, I _{OH} =4.0mA	3.9	4.2		V
L-level output voltage	V _{OL}		V _{DD} =4.5V, I _{OL} =4.0mA		0.3	0.5	
Output leak current	I _Z	Q pin, Fig. 1, INH pin="L", V _{DD} =5.5V	V _{OH} =V _{DD} , V _{OL} =V _{SS}			10	μA
H-level input voltage	V _{IH}	INH pin		2.0			
L-level input voltage	V _{IL}					0.8	
Current consumption	I _{DD1}	Load circuit 1, Fig. 2, Cl=15pF, INH=OPEN, f=30MHz	SM5619H1		11	20	mA
			SM5619H3		8	14	
			SM5619H5		6	11	
			SM5619H7		5	9	
Pull-up resistor	R _{UP}	INH pin, Fig. 3		50		250	kΩ
Feedback resistor	R _f	Fig. 4		90	100	110	kΩ
Inverter amplifier output resistor	R _D	Calculated from R _f		740	820	900	Ω
Internal capacitor	C _G			18.9	21	23.1	pF
	C _D			18.9	21	23.1	

■ SWITCHING CHARACTERISTICS

1. N series

($V_{DD} = 5 \pm 0.5$ V, $V_{SS} = 0$ V and $T_a = -20$ to $+80^\circ\text{C}$ unless otherwise specified)

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Output rise time	T_r	Load circuit 1, Fig. 2 $0.1V_{DD}$ to $0.9V_{DD}$	$C_L=15\text{pF}$	2.0	4.0	ns
			$C_L=50\text{pF}$	4.0	8.0	
Output fall time	T_f	Load circuit 1, Fig. 2 $0.9V_{DD}$ to $0.1V_{DD}$	$C_L=15\text{pF}$	2.0	4.0	ns
			$C_L=50\text{pF}$	4.0	8.0	
Output duty cycle	DUTY	Load circuit 1, Fig. 2, $V_{DD}=5.0$ V, $T_a=25^\circ\text{C}$, $C_L \leq 50\text{pF}$	45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, $V_{DD}=5.0$ V,			100	ns
Output enable delay time	T_{PZL}	$T_a=25^\circ\text{C}$, Load $C_L \leq 50\text{pF}$			100	
Maximum operating frequency	f_{MAX}	Load circuit 1, Fig. 2, $C_L=50\text{pF}$, Checked with lot monitor	30			MHz

2. H series

($V_{DD} = 5 \pm 0.5$ V, $V_{SS} = 0$ V and $T_a = -20$ to $+80^\circ\text{C}$ unless otherwise specified)

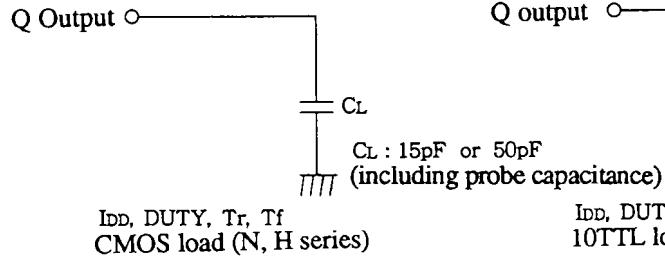
ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Output rise time	T_r	Load circuit 1, Fig. 2 $0.1V_{DD}$ to $0.9V_{DD}$, $C_L=15\text{pF}$		5.0	10	ns
Output fall time	T_f	Load circuit 1, Fig. 2 $0.9V_{DD}$ to $0.1V_{DD}$, $C_L=15\text{pF}$		5.0	10	ns
Output duty cycle	DUTY	Load circuit 1, Fig. 2, $V_{DD}=5.0$ V, $T_a=25^\circ\text{C}$, $f=30\text{MHz}$, $C_L=50\text{pF}$	45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, $V_{DD}=5.0$ V, $T_a=25^\circ\text{C}$,			100	ns
Output enable delay time	T_{PZL}	Load $C_L \leq 15\text{pF}$			100	
Maximum operating frequency	f_{MAX}	Load circuit 1, Fig. 2, $C_L=15\text{pF}$, Checked with lot monitor	30			MHz

3. K1 version

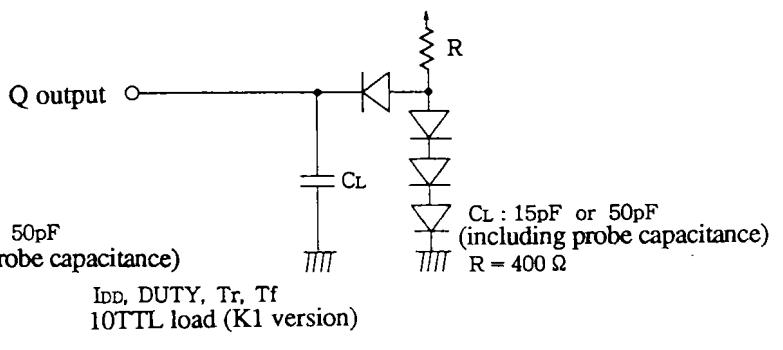
($V_{DD} = 5 \pm 0.5$ V, $V_{SS} = 0$ V and $T_a = -20$ to $+80^\circ\text{C}$ unless otherwise specified)

ITEM	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Output rise time	T_r	Load circuit 2, Fig. 2 $0.4V$ to $2.4V$, $C_L=15\text{pF}$		2.0	4.0	ns
Output fall time	T_f	Load circuit 2, Fig. 2 $2.4V$ to $0.4V$, $C_L=15\text{pF}$		2.0	4.0	ns
Output duty cycle	DUTY	Load circuit 2, Fig. 2, $V_{DD}=5.0$ V, $T_a=25^\circ\text{C}$, $f=30\text{MHz}$, $C_L=15\text{pF}$	45		55	%
Output disable delay time	T_{PLZ}	Fig. 2, $V_{DD}=5.0$ V, $T_a=25^\circ\text{C}$,			100	ns
Output enable delay time	T_{PZL}	Load $C_L \leq 15\text{pF}$			100	
Maximum operating frequency	f_{MAX}	Load circuit 2, Fig. 2, $C_L=15\text{pF}$, Checked with lot monitor	30			MHz

■ LOAD CIRCUIT



Load circuit 1



Load circuit 2

■ MEASURING CIRCUIT

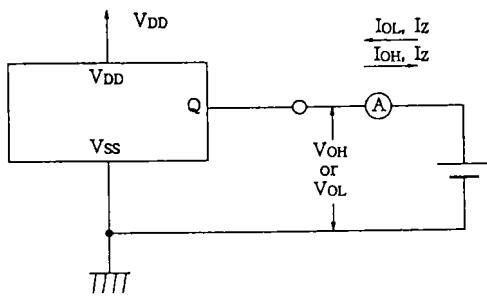


Figure 1

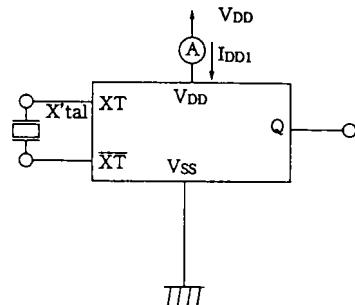


Figure 2

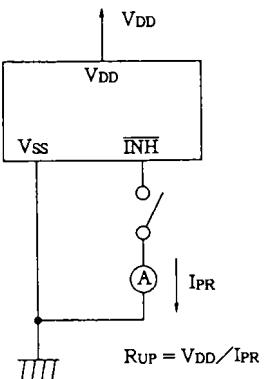


Figure 3

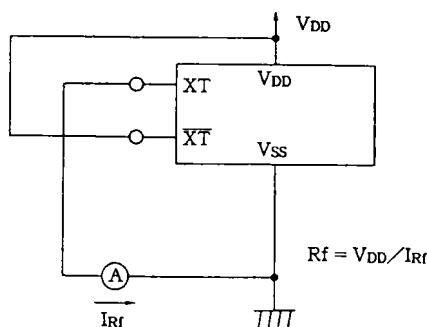
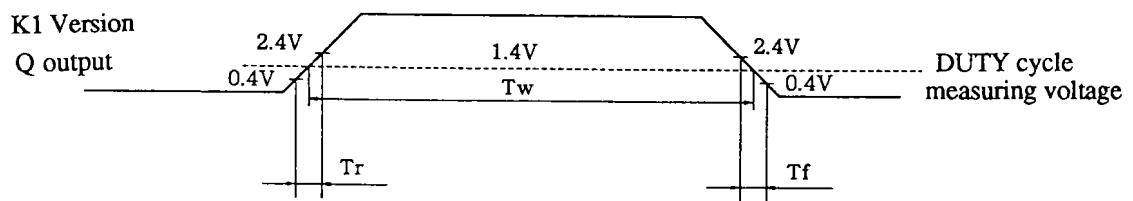
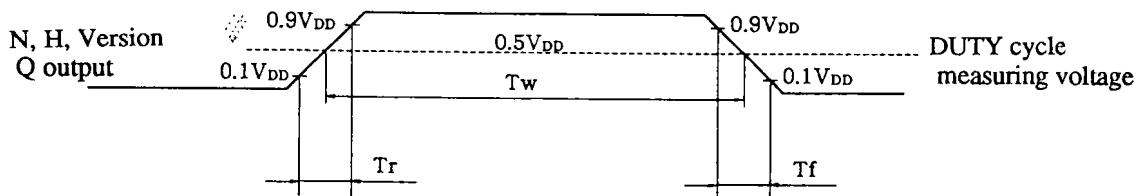
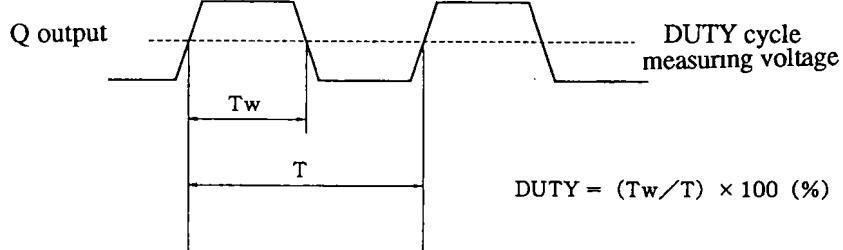


Figure 4

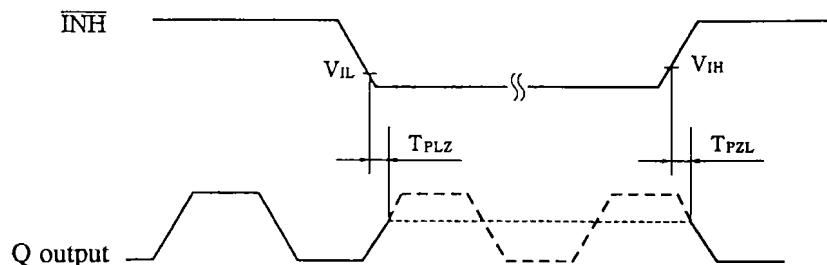
■ SWITCHING TIME WAVEFORM



■ OUTPUT DUTY CYCLE TIME

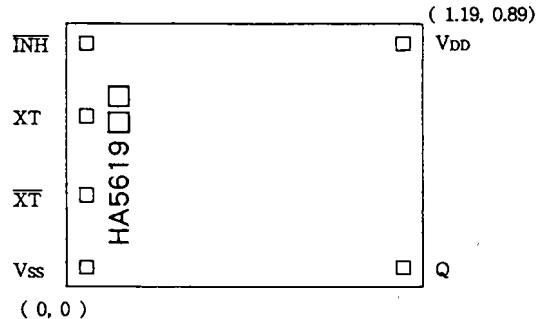


■ OUTPUT DISABLE DELAY TIME, OUTPUT ENABLE DELAY TIME V_{IL}



Q output, INH input waveform Tr = Tf 10 ns or less

■ PAD LAYOUT



Chip size: $1.19 \times 0.89\text{mm}$

Chip thickness: $400 \pm 30 \mu\text{m}$

* **□ □** version name

■ PAD COORDINATES (Unit: μm)

Pin name	X	Y
INH	183.5	707.5
XT	183.5	517.5
XT̄	183.5	327.5
VSS	183.5	137.5
Q	1042.5	141.5
VDD	1042.5	742.5

Step number	S5	S4	S3	S2	S1	S0
63	HIGH	HIGH	HIGH	HIGH	LOW	LOW
⋮	⋮	⋮	⋮	⋮	⋮	⋮
36	HIGH	LOW	LOW	LOW	LOW	HIGH
35	HIGH	LOW	LOW	LOW	LOW	LOW
34	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
⋮	⋮	⋮	⋮	⋮	⋮	⋮
5	LOW	LOW	LOW	LOW	HIGH	LOW
4	LOW	LOW	LOW	LOW	LOW	HIGH
3	LOW	LOW	LOW	LOW	LOW	LOW

Note

Pins S0 to S5 have internal pull-up resistances. Therefore, only LOW-level pins need be tied to ground. However, it is recommended that HIGH-level inputs be tied to VDD for applications using fixed-length shifting.

Input/Output Control

Inputs				Shift register (internal)	Outputs	
RSTN	ENRC	CLK	OE		OUT0 to OUT7	
x	x	x	LOW			High impedance
x	x	x	HIGH			Enable
HIGH	HIGH	LOW-to-HIGH	x	Rotate shift		
HIGH	LOW	LOW-to-HIGH	x	Non-rotate shift		
LOW	x	x	x	Reset		

Note

x = don't care